

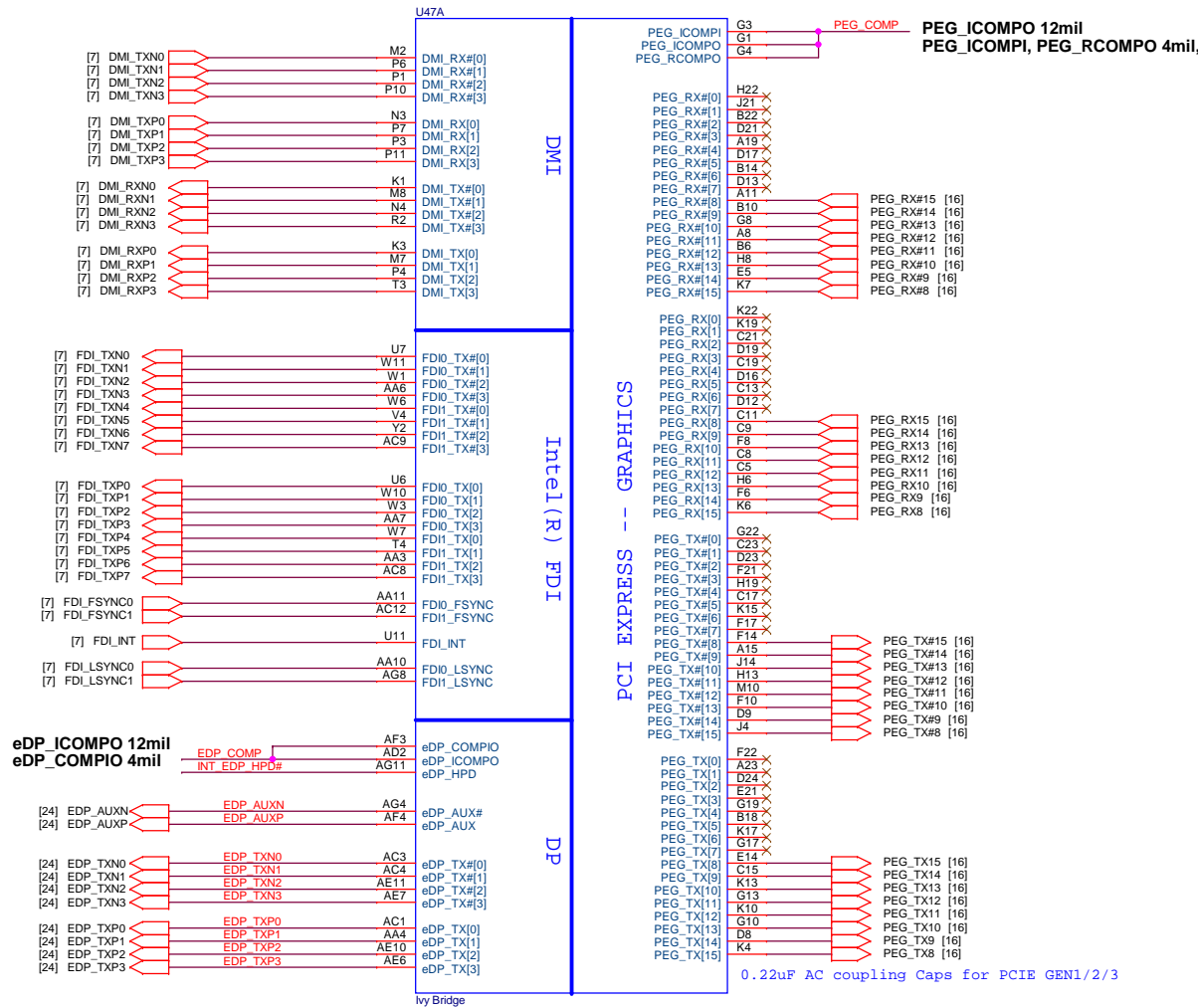




# Ivy Bridge Processor (DMI,PEG,FDI) (CPU)

02

PEG\_ICOMPI and RCOMPO signals should be shorted and routed with  
- max length = 500 mils  
- typical impedance = 43 mohms  
PEG\_ICOMPO signals should be routed with  
- max length = 500 mils  
- typical impedance = 14.5 mohms

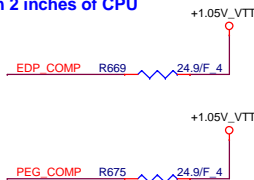


DP\_COMPIO and ICOMPO signals should be shorted near balls and routed with  
- typical impedance < 25 mohms

DG 1.0 :  
The recommended AC cap value is changed to 220nF for compatibility with PCIe Gen3 on future platforms.  
For Gen2 only designs, it is acceptable to continue to use the 100nF capacitor.

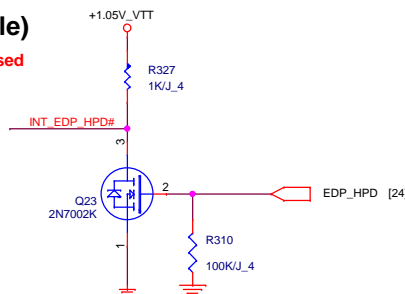
## DP & PEG Compensation

CAD Note: Place PU resistor within 2 inches of CPU



## eDP Hot-plug (Disable)

HPD PU/PD resistor values based on CRB and different to DG



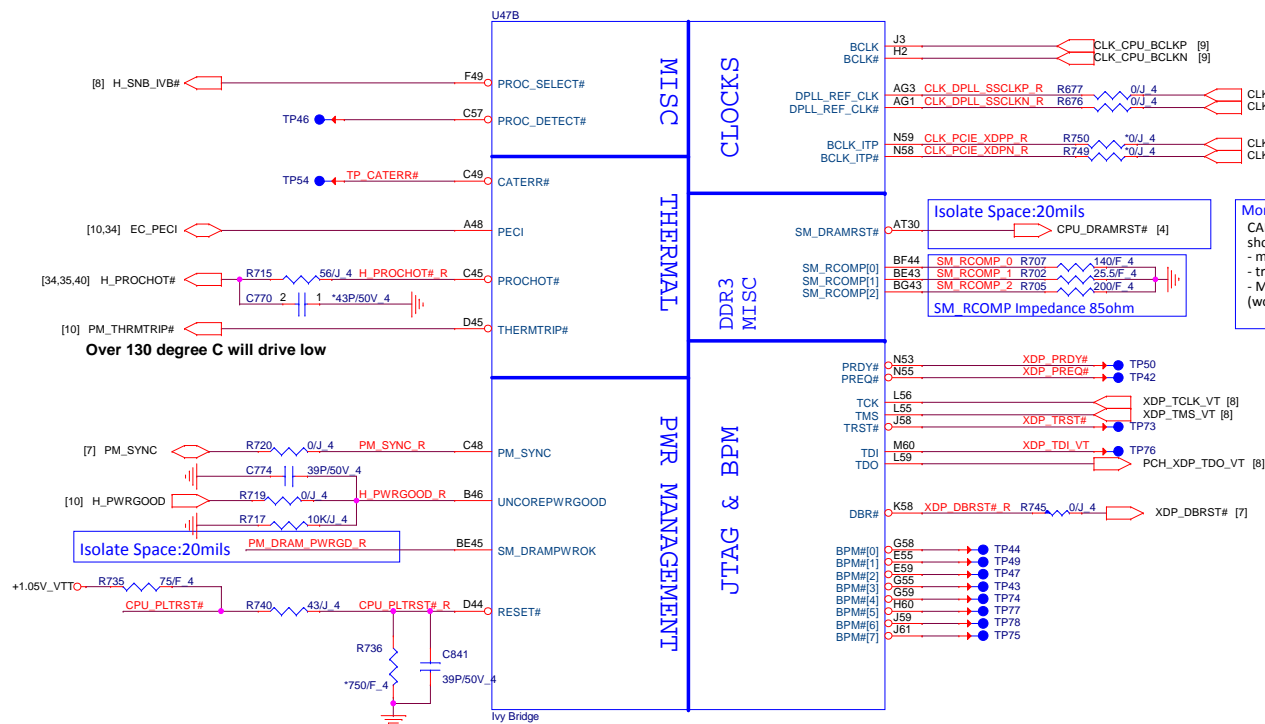
Quanta Computer Inc.

PROJECT : ZQK

Size	Document Number	Rev
	Ivy Bridge 1/5 (HOST & PCIE)	1A
Date:	Monday, January 07, 2013	Sheet 2 of 46



## Ivy Bridge Processor (CLK,MISC,JTAG) (CPU)



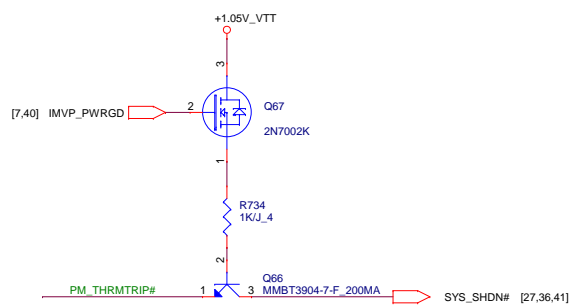
If motherboard only supports external graphics or if it supports Processor Graphics but without vGP, Connect DPLL\_REF\_SSCLK on Processor to GND through 1K +/- 5% resistor. Connect DPLL\_REF\_SSCLK on Processor to VCCP through 1K +/- 5% resistor.

05/15 : PCH\_XDP\_TDO\_VT already pull high +3V\_S5 on PCH side

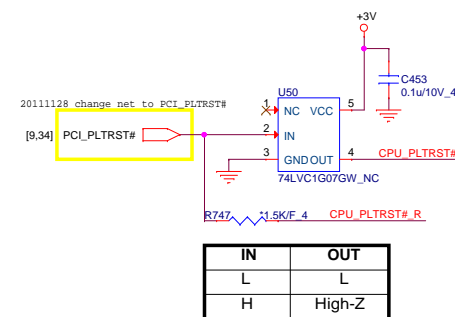
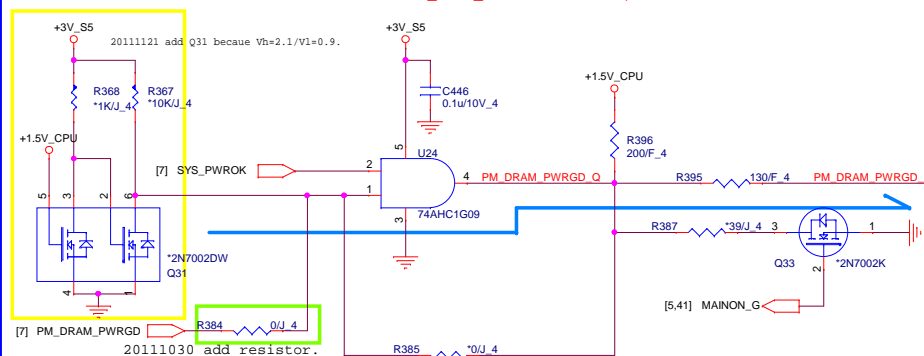
68 ohm for unused, 62 ohm for used

When MP, JTAG PU/PD resistor can be removed? (Yes Intel, TDI, TDO, TMS, TRST#, TCK, PREQ#, PRDY#)

## Thermal Trip (CPU)



## S3 leakage circuit (CPU)



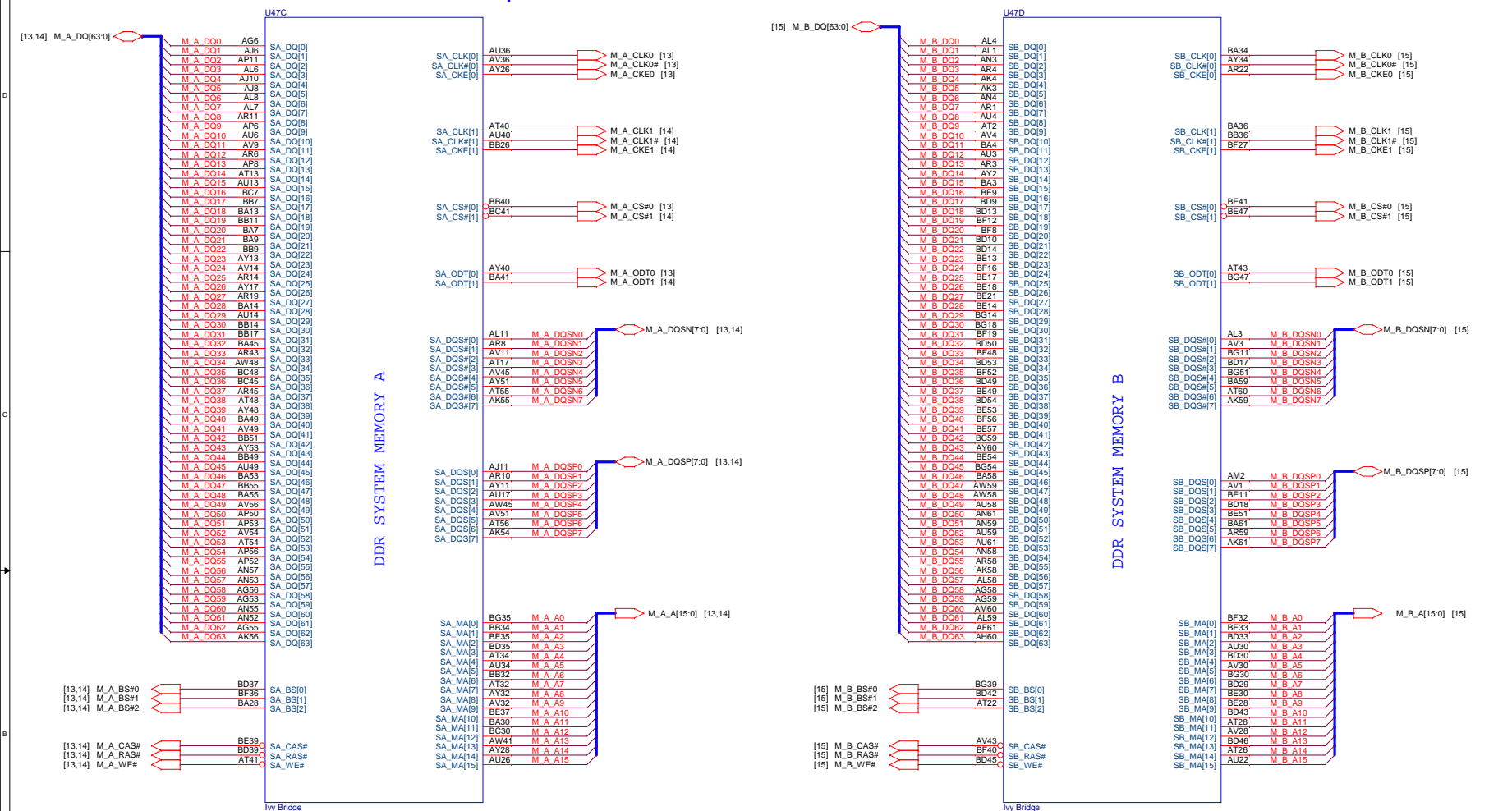
**Quanta Computer Inc.**  
PROJECT : ZQK

Size Document Number  
Ivy Bridge 2/5 (CLK & JTAG)  
Date: Monday, January 07, 2013 Sheet 3 of 46 Rev 1A



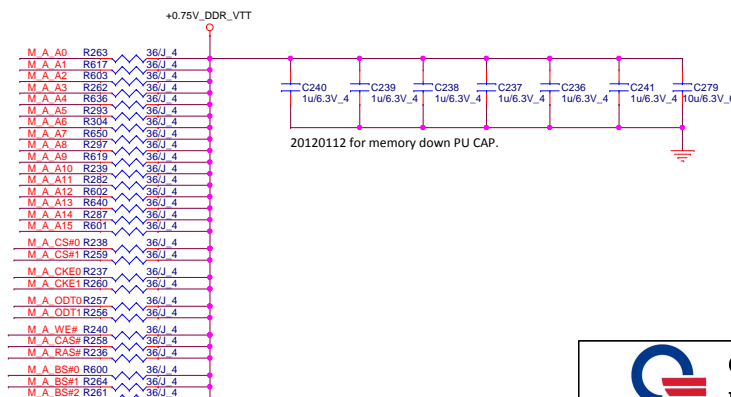
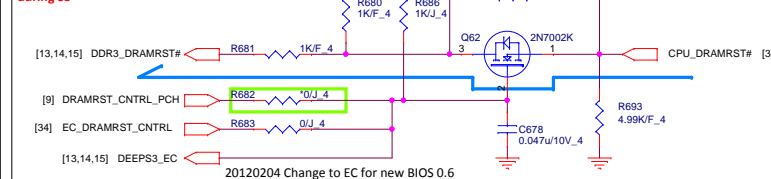
**Channel A: On board RAM 2Rx16 8pcs**

### Channel B: SO-DIMM



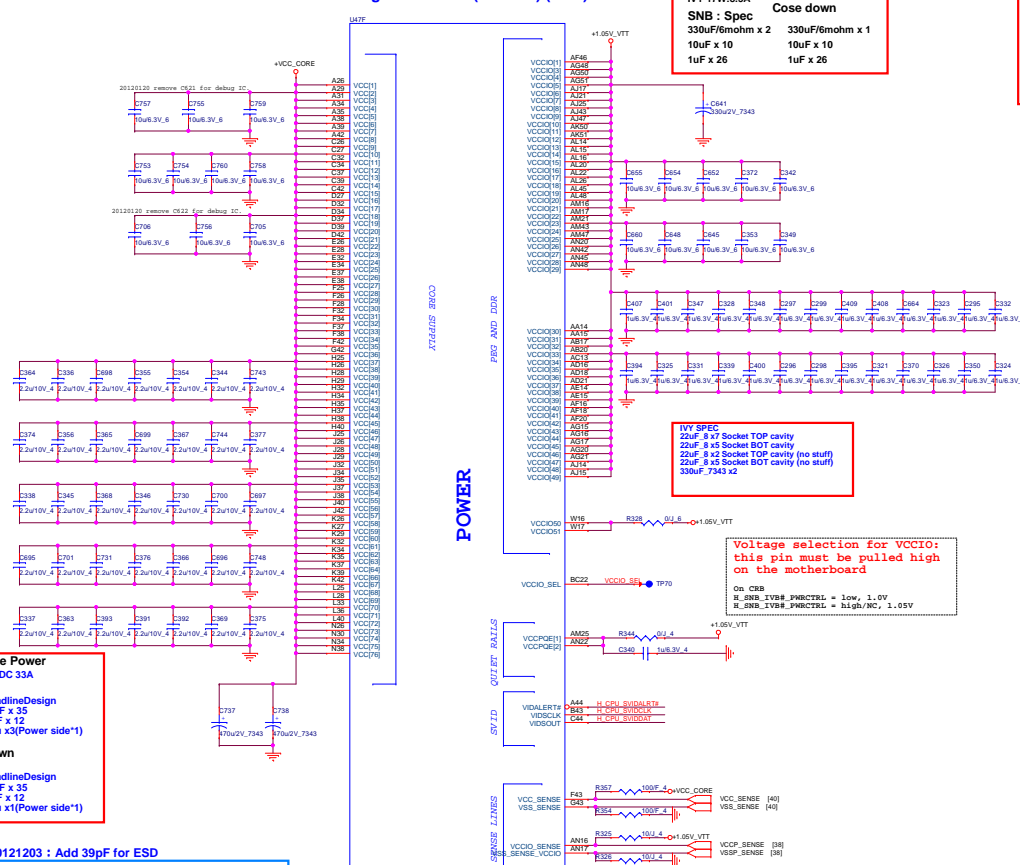
### S3 leakage circuit (CPU)

**S3 circuit: DRAM\_RST# to memory should be high during S3**

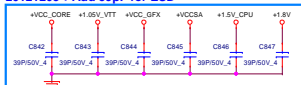




IVY Bridge Processor (POWER) (CPU)



0121203 : Add 39pF for ESD



Note: need routing  
for and ALERT need  
CLK and DATA



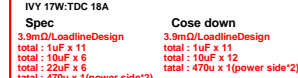
Place PU resistor close to CPU



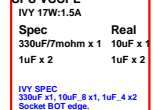
Place PU resistor close to CPL



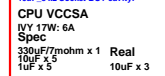
## CPU VCCAXG



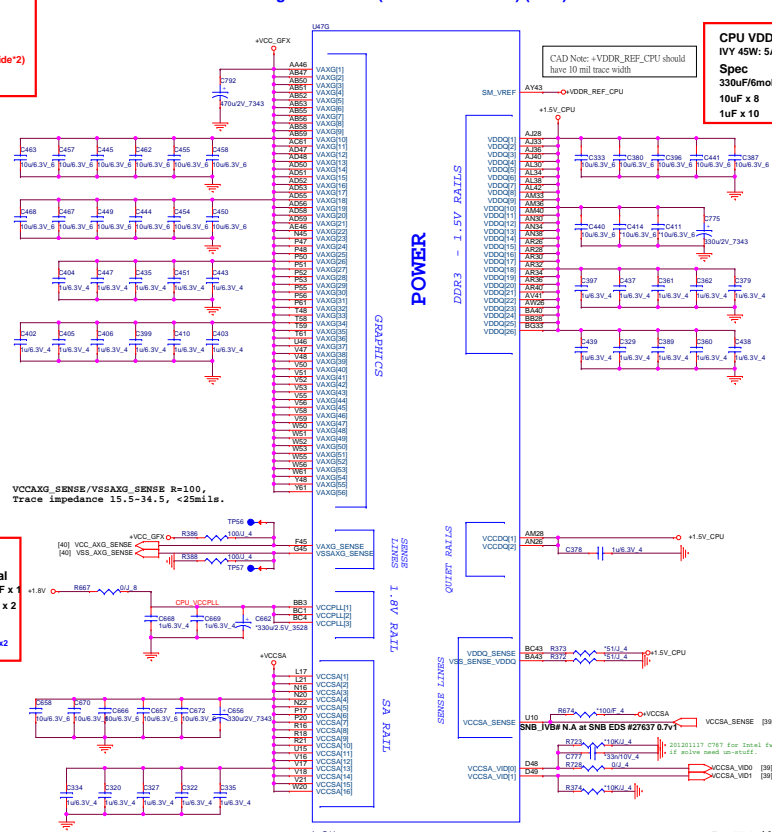
## CPU VCCF



**IVY SPEC**  
330uF x1, 10uF\_8 x1 Socket BOT edge  
10uF\_8 x2 Socket BOT cavity.



## IVY Bridge Processor (GRAPHIC POWER) (CPU)



For IV Bridge

VID[0]	VID[1]	+VCCSA
0	0	0.9V
0	1	0.8V
1	0	0.725V
1	1	0.675V

For SN Bridge

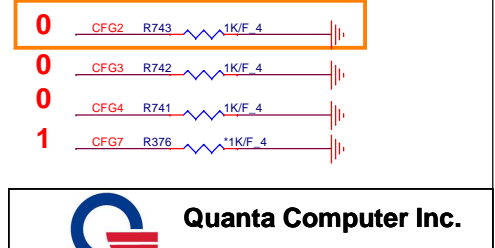
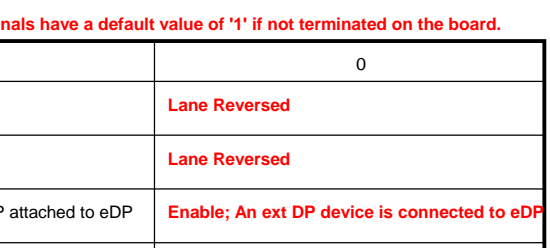
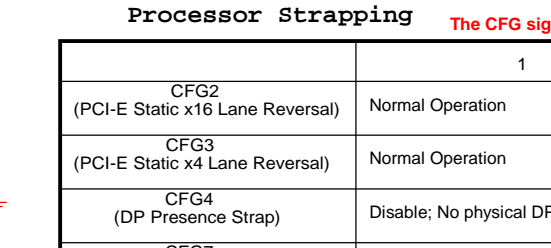
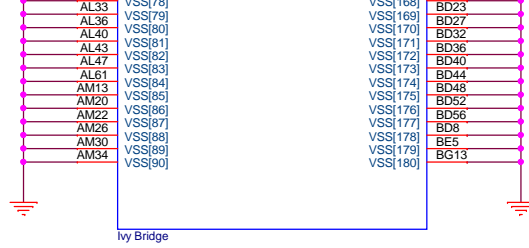
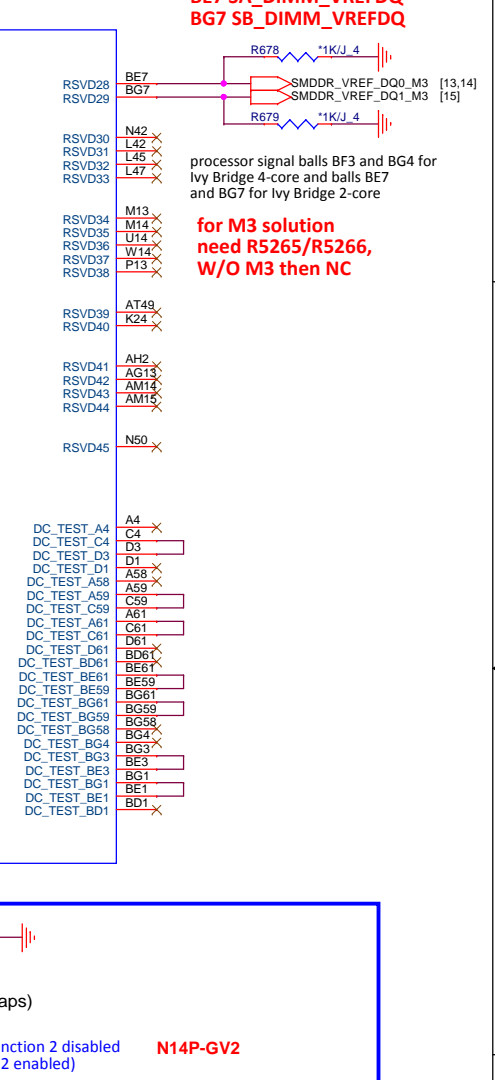
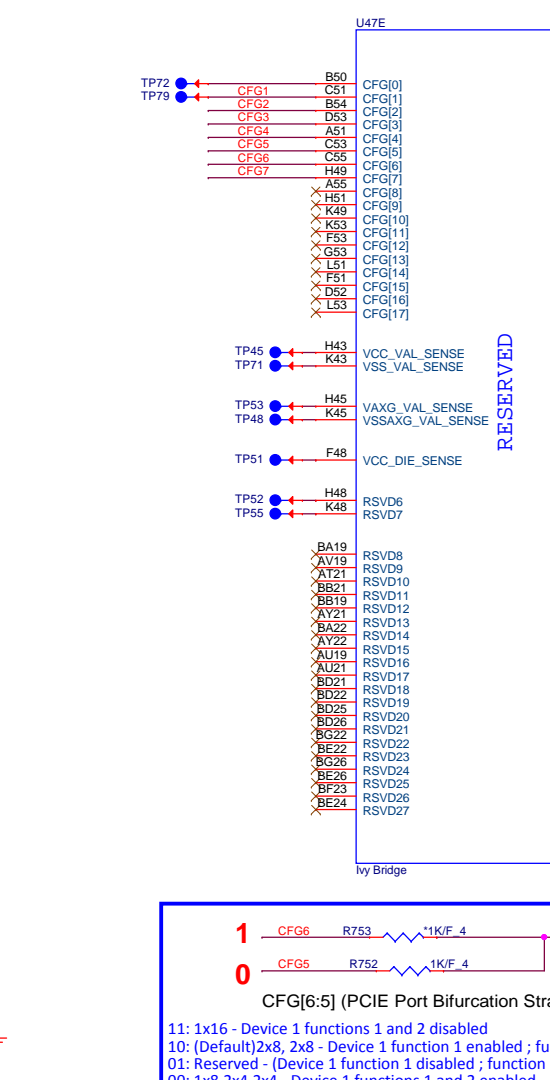
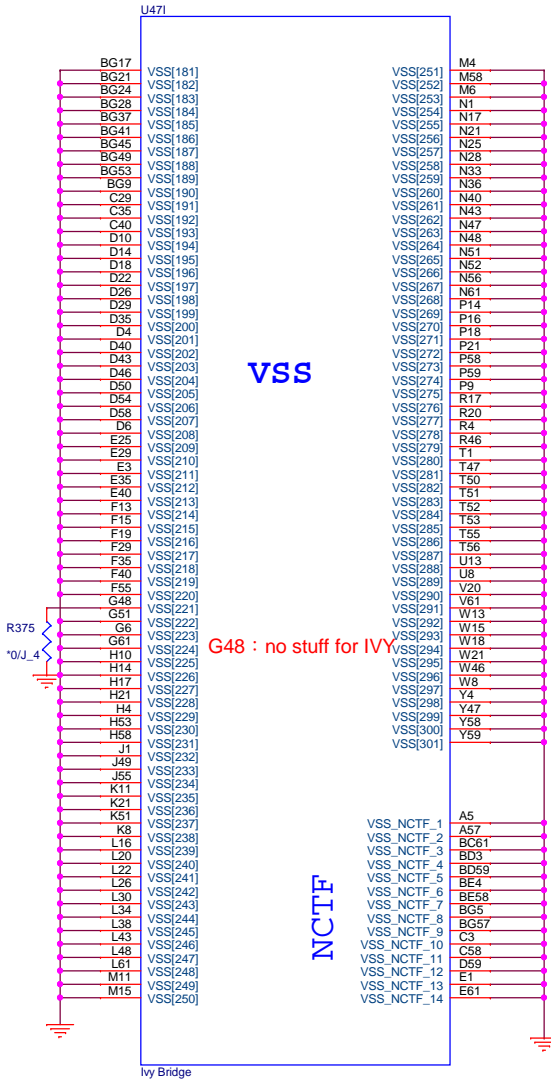
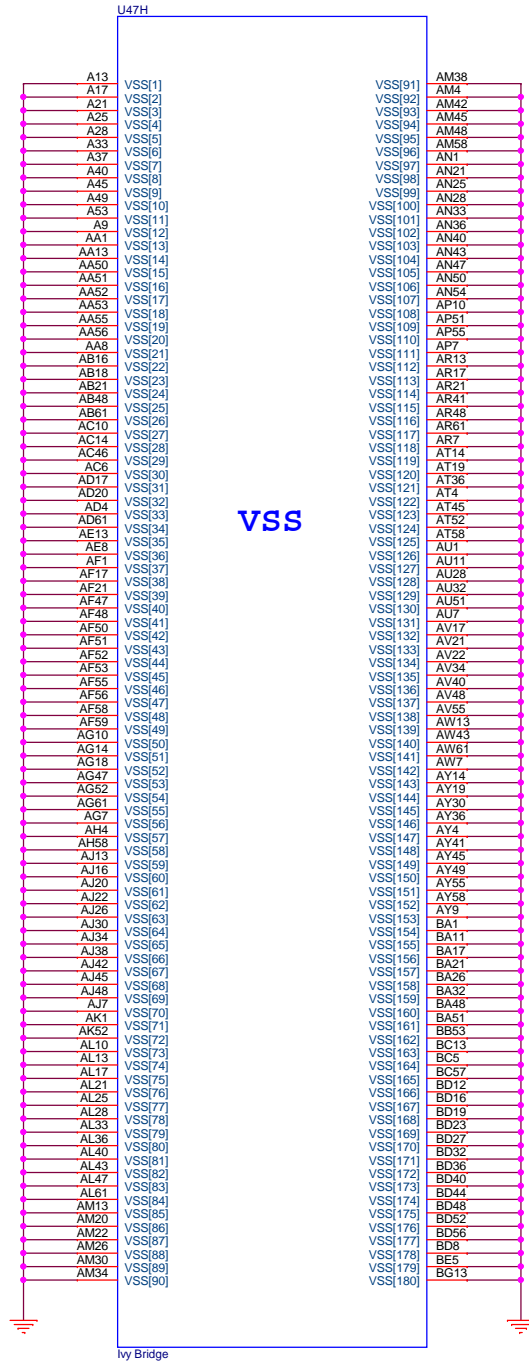
VID[1]	+VCCSA
0	0.9V
1	0.8V



IVY Bridge Processor (GND) (CPU)

IVY Bridge Processor (RESERVED, CFG) (CPU)

BE7 SA\_DIMM\_VREFDQ  
BG7 SB\_DIMM\_VREFDQ



Processor Strapping		The CFG signals have a default value of '1' if not terminated on the board.	
CFG2 (PCI-E Static x16 Lane Reversal)	Normal Operation	Lane Reversed	
CFG3 (PCI-E Static x4 Lane Reversal)	Normal Operation	Lane Reversed	
CFG4 (DP Presence Strap)	Disable; No physical DP attached to eDP	Enable; An ext DP device is connected to eDP	
CFG7 (PEG Defer Training)	PEG train immediately following xxRESETB de assertion	PEG wait for BIOS training	

0 CFG2 R743 1K/F 4

0 CFG3 R742 1K/F 4

0 CFG4 R741 1K/F 4

1 CFG7 R376 1K/F 4

Quanta Computer Inc.

PROJECT : ZQK

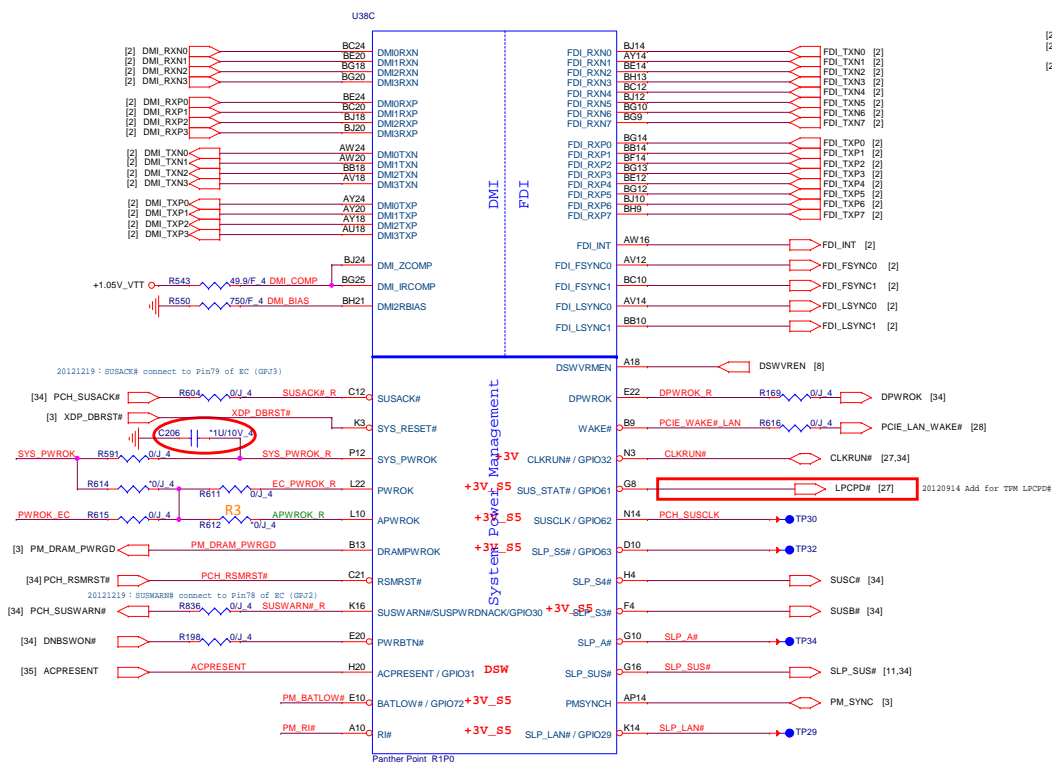
Ivy Bridge 5/5 (GND)

Size Document Number Rev 1A

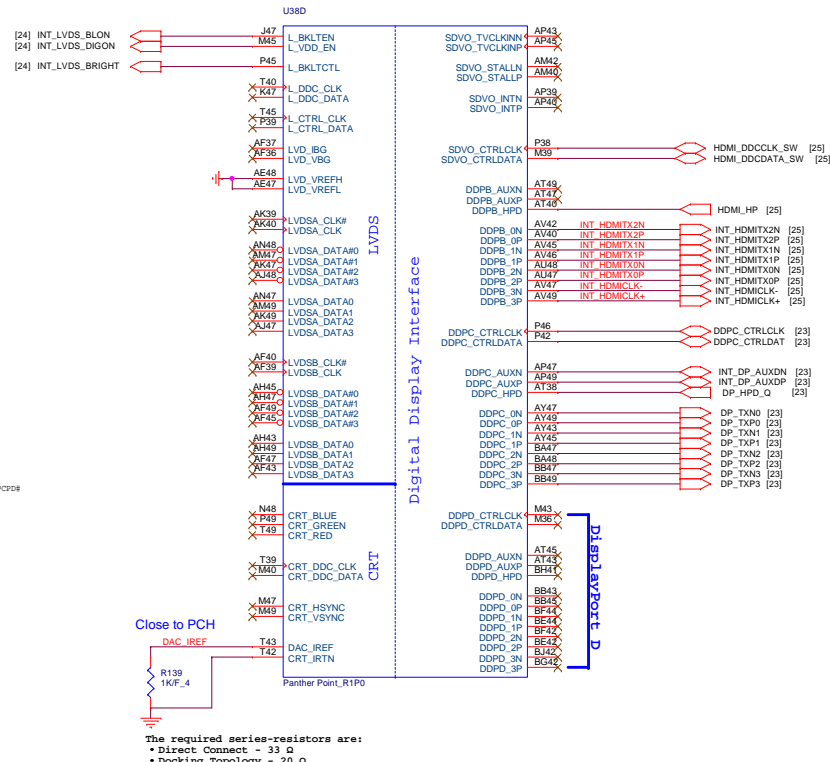
Date: Monday, January 07, 2013 Sheet 6 of 46



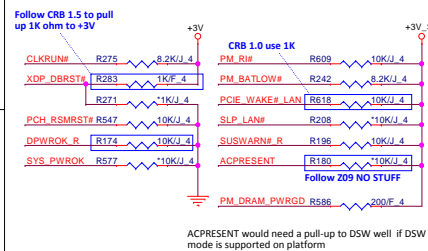
**CPT/PPT (DMI,FDI,PM) (CLG)**



### CPT/PPT (LVDS,DDI)

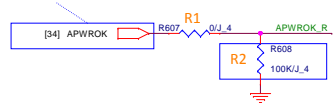


### PCH Pull-high/low (CLG)

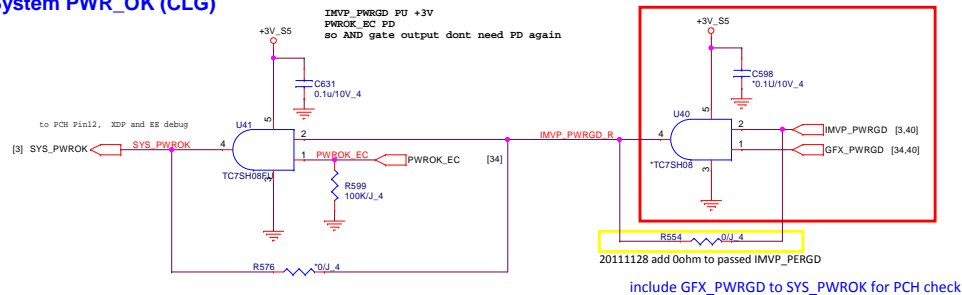


20120706:Speed up 250ms to boot up  
R1,R2,R3 for EC power on 250 ms

20121004(EC Anda) : Chage trigger pin from +0.75V\_ON to APWROK ; R2 change to 100K

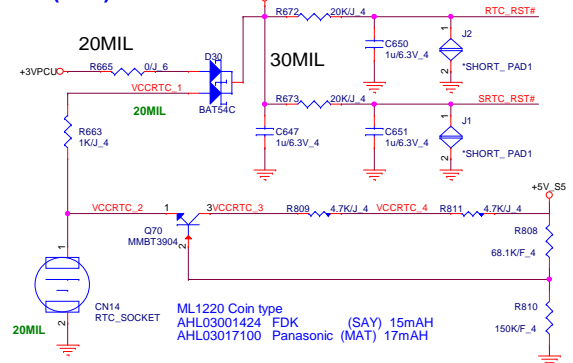


## System PWR\_OK (CLG)

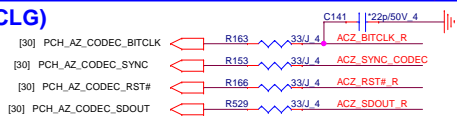




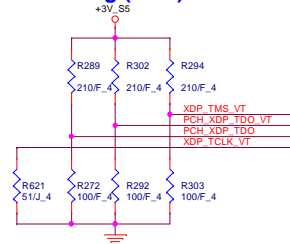
## RTC (RTC)



## HDA Bus (CLG)

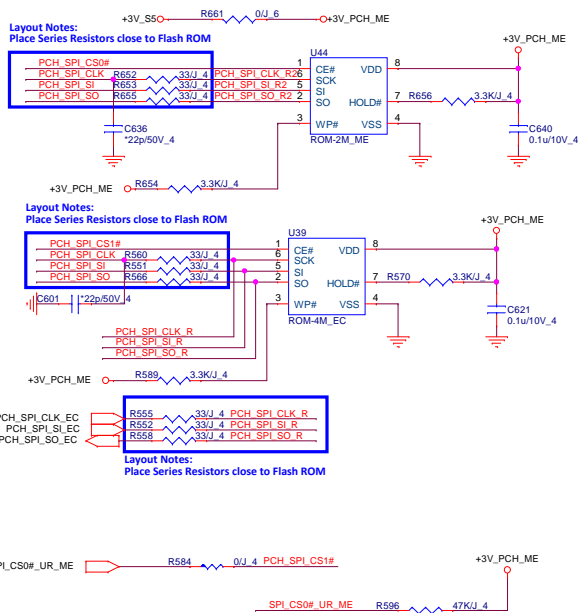


## PCH JTAG Debug (CLG)

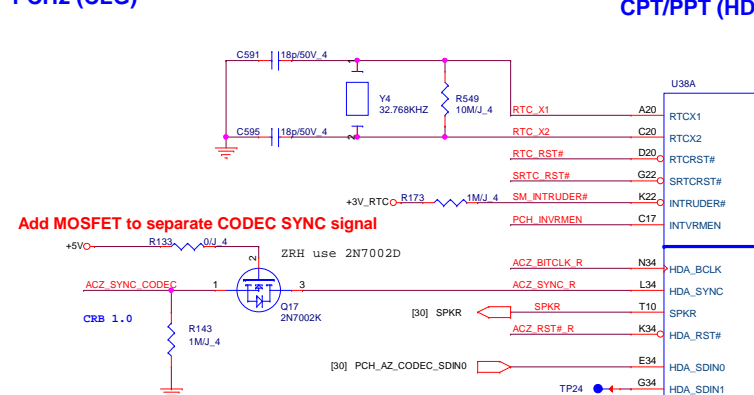


### PCH Dual SPI (CLG) (Default for WIN8)

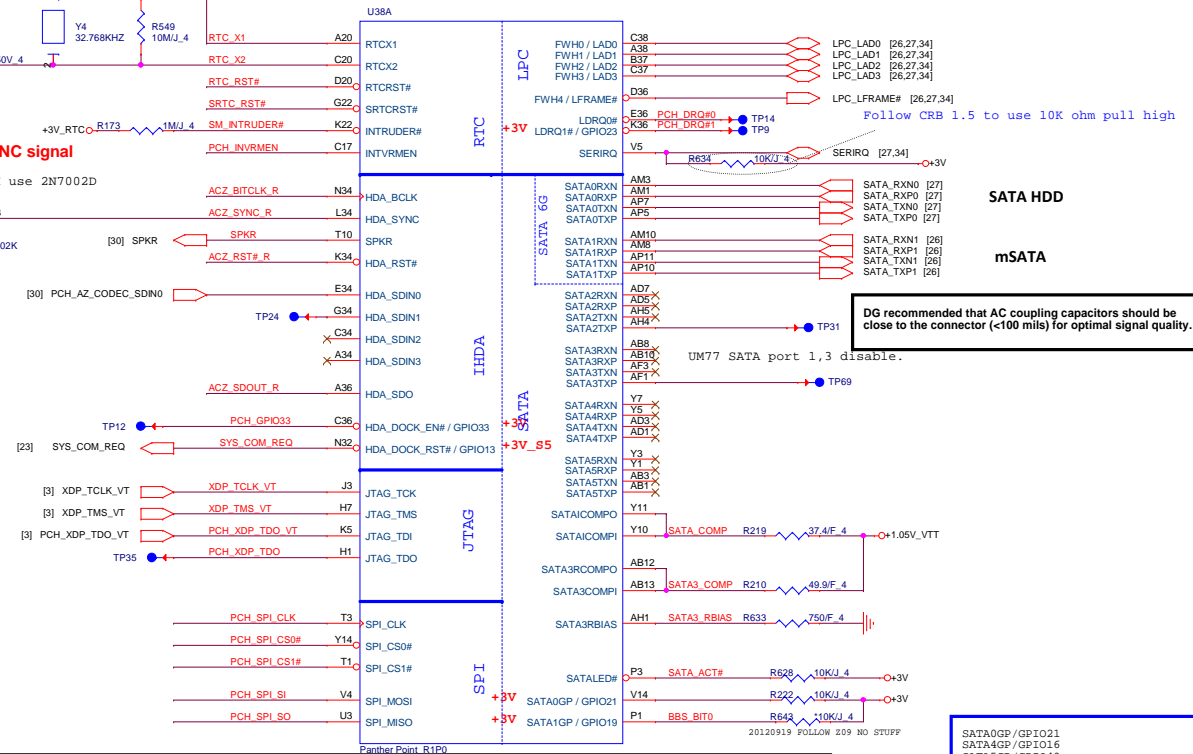
```
W25Q32BVSSIG / AKE391P0N00----->4MB
W25Q16BVSSIG / AKE38FP0N01----->2MB
```



## PCH2 (CLG)



### CPT/PPT (HDA,JTAG,SATA) (CLG)



### PCH Strap Table

Pin Name	Strap description	Sampled	Configuration										
SPKR	No reboot mode setting	PWROK	0 = Default (weak pull-down 20K) 1 = Setting to No-Reboot mode										
GNT3# / GPIO55	Top-Block Swap Override	PWROK	0 = "top-block swap" mode 1 = Default (weak pull-up 20K)										
INTVRMEN	Integrated 1.05V VRM enable	ALWAYS	Should be always pull-up										
GNT1# / GPIO51	Boot BIOS Selection 1 [bit-1]	PWROK	<table border="1"><thead><tr><th>GNT1#</th><th>GPIO19</th><th>Boot Location</th></tr></thead><tbody><tr><td>1</td><td>1</td><td>SPI *</td></tr><tr><td>0</td><td>0</td><td>LPC</td></tr></tbody></table>	GNT1#	GPIO19	Boot Location	1	1	SPI *	0	0	LPC	
GNT1#	GPIO19	Boot Location											
1	1	SPI *											
0	0	LPC											
GPIO19	Boot BIOS Selection 0 [bit-0]	PWROK											
HDA_SDO	Flash Descriptor Security	RSMRST	0 = effect (default)(weak pull-down 20K) 1 = overridden										
DF_TVS	DMV/FDI Termination voltage	PWROK	0 = Set to Vss (weak pull-down 20K) 1 = Set to Vcc										
GPIO28	On-die PLL Voltage Regulator	RSMRST#	0 = Disable 1 = Enable (weak pull-up 10K)										
HDA_SYNC	On-Die PLL VR Voltage Select	RSMRST	0 = Support by 1.8V (weak pull-down) 1 = Support by 1.5V										
GPIO15	Intel ME Crypto Transport Layer Security (TLS) cipher suite internal PD	RSMRST	0 = Disable (Default) 1 = Enable										
DSWVREN	DEEP S4/S5 well On Die DSW VR Enable	DSW	High = Enable (Default) Low = Disable										
NV_ALE	Intel Anti-Theft HDD protection Only for Interposer	PWROK	0 = Disable (Internal pull-down 20kohm)										

Used as GPIO only. at chklist 1.2

**Default weak pull-up on GNT0/1#**  
[Need external pull-down for LPC BIOS]

ME\_WR default EC setting folating

for future CPU, Sandy Bridge NC  
DF\_TVS needs to be pulled up to VccDFTERM power rail  
through 2.2 kOhm  $\pm 5\%$  - R8361 change to 0 or not??

Needs to be pulled High for Chief River platform  
chklist 2.0



## CPT/PPT (PCI,USB,NVRAM) (CLG)

## CPT/PPT (PCI-E,SMBUS,CLK)

U3B8

2011122 add for Touch pad interrupt pin from GPIO13 to GPIO11.

PCIe port 1 for commercial model S3 can't weak up.

Wireless

LAN

UM77/HM70 will disable 5-8 PCIe ports

EHC1

EHC2

20110908 WLAN support S3 wake up function.

Wireless

LAN

## CLK\_REQ/Strap Pin(CLG)

## SMBus(EC) (CLG)

## SMBus(PCH) (CLG)

Layout Notes:  
USB3 TX AC cap place at connector side, AC cap to  
connector < 400nfs

## USB30 Port1: EXT USB3.0 Port

## USB30 Port3: Mini DP port

## USB3.0

## USB2.0

## USB

## USB

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## PLTRST#(CLG)

## PCI/USB0# Pull-up(CLG)

## DDR3 Memory down strap (CLG)

Vendor	RAM_ID#	Q PW	Mér. PN	Freq.
Hynix	0000			
Elpida	0001	AKD5JGS7400	EDJ4216EBB0-DJ-F	1333MHz
	0010	AKD5JGS7407	EDJ4216EPB0-GNL-F	1600MHz

## EV@: For Optimize SKU

## IV@: For UMA SKU

## MPC Switch Control

MPC\_PWR\_CTRL#

MPC\_PWR\_CTRL#

MPC\_PWR\_CTRL#

MPC\_PWR\_CTRL#

MPC\_PWR\_CTRL#

MPC\_PWR\_CTRL#

MPC\_PWR\_CTRL#

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MPC\_PWR\_CTRL#

MPC\_PWR\_CTRL#

## EV@: For Optimize SKU

## IV@: For UMA SKU

## MPC Switch Control

MPC\_PWR\_CTRL#

MPC\_PWR\_CTRL#

MPC\_PWR\_CTRL#

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MPC\_PWR\_CTRL#

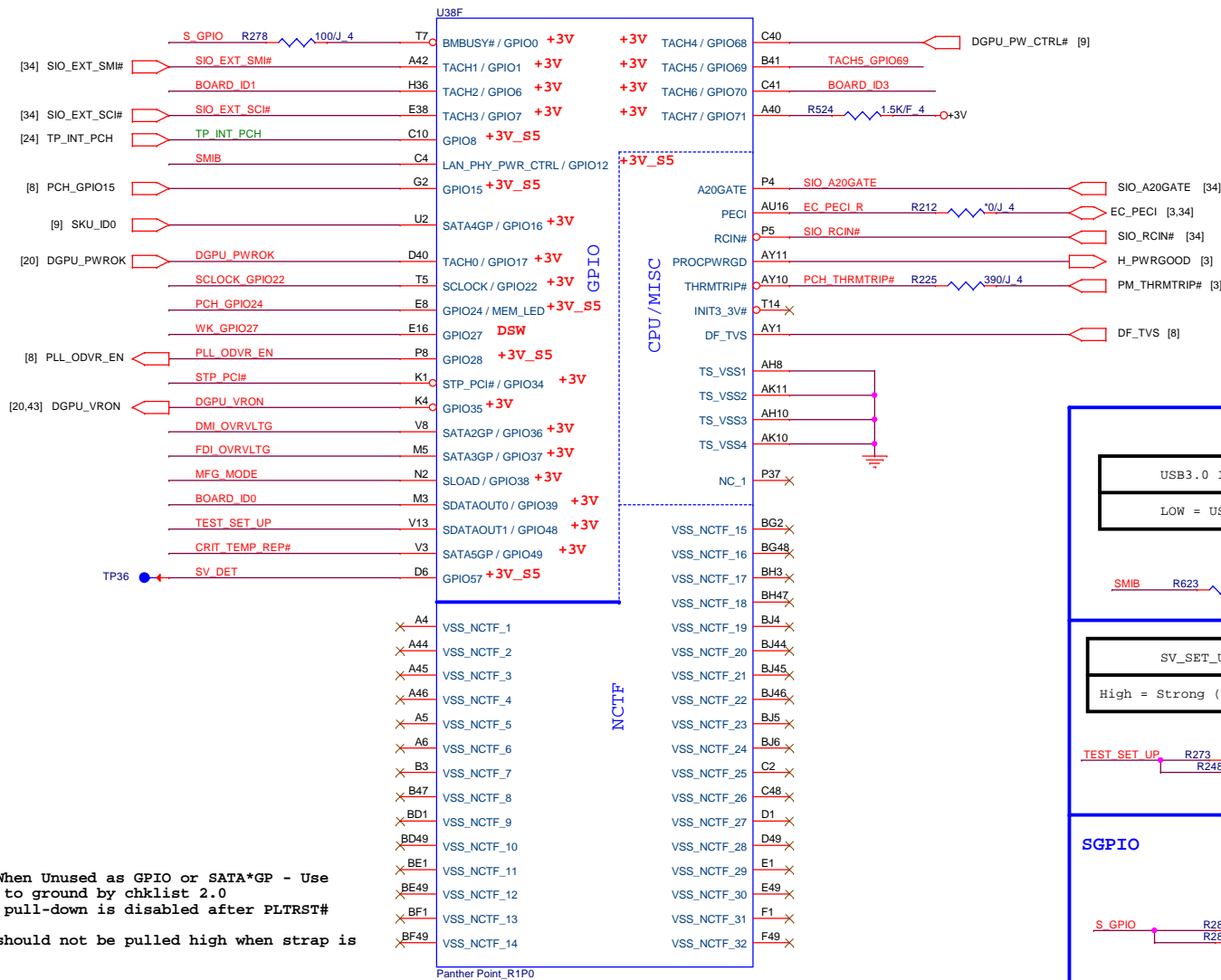
1 = GPU power is control by H/W (pure Discrete SKU)

0 = GPU power is control by PCH GPIO (Discrete, SG or Optimize)

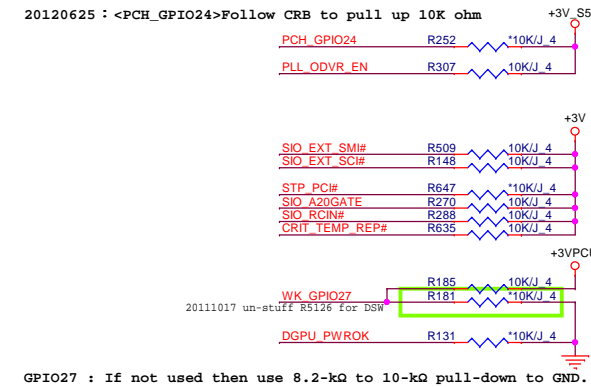


## CPT/PPT (GPIO,VSS\_NCTF,RSVD) (CLG)

10



## GPIO Pull-up/Pull-down (CLG)



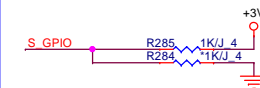
USB3.0 IC CTL

LOW = USB3.0 IC

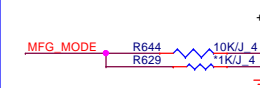
SV\_SET\_UP

High = Strong (Default)

## SGPIO

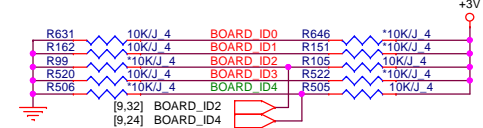
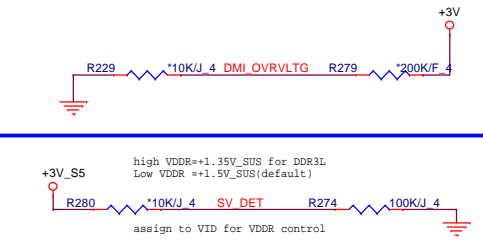


## MFG-TEST



DMI TERMINATION VOLTAGE OVERRIDE

Low = Tx, Rx terminated to same voltage (DC Coupling Mode) (DEFAULT)



	High	Low
BOARD_ID0	GDDR5	DDR3
BOARD_ID1	Disable on board memory	Enable on board memory
BOARD_ID2	Pin8 of SYNAPTICS and ELAN are NC pin	
	Default is pull high	
	BIOS maybe will use EEPROM detection	
BOARD_ID3		
BOARD_ID4	No touch panel	Touch panel

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PROJECT : ZQK

PCH 4/6 (GPIO/MISC)

Size Document Number Rev 1A

Date: Monday, January 07, 2013 Sheet 10 of 46

2011/09/01 add select resistor

LVDS = Pull HIGH

eDP = Pull LOW

20120607 : follow CRB pull down

FDI TERMINATION VOLTAGE OVERRIDE

LOW - Tx, Rx terminated to same voltage

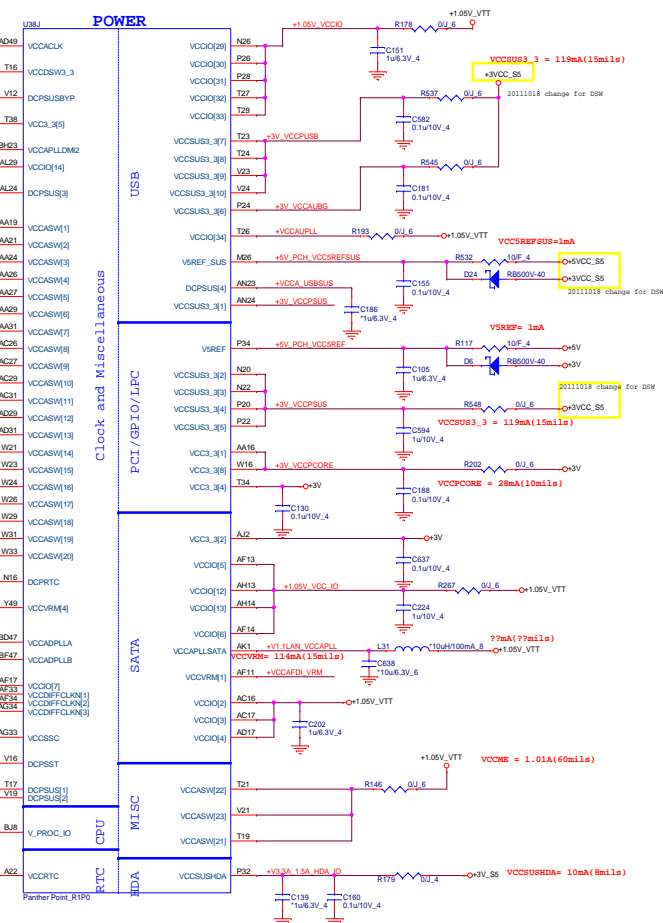
G\_SENSOR\_ID

High = Disable (Default)

Low = Enable

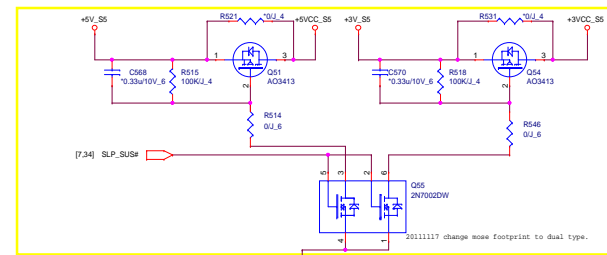
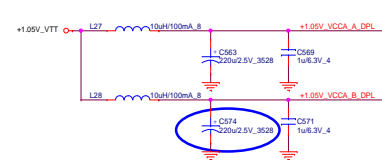
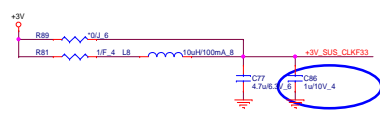
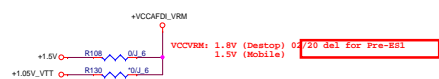


CPT/PPT (POWER) (CLG)



20120105 change power plant to +3V for power saving.

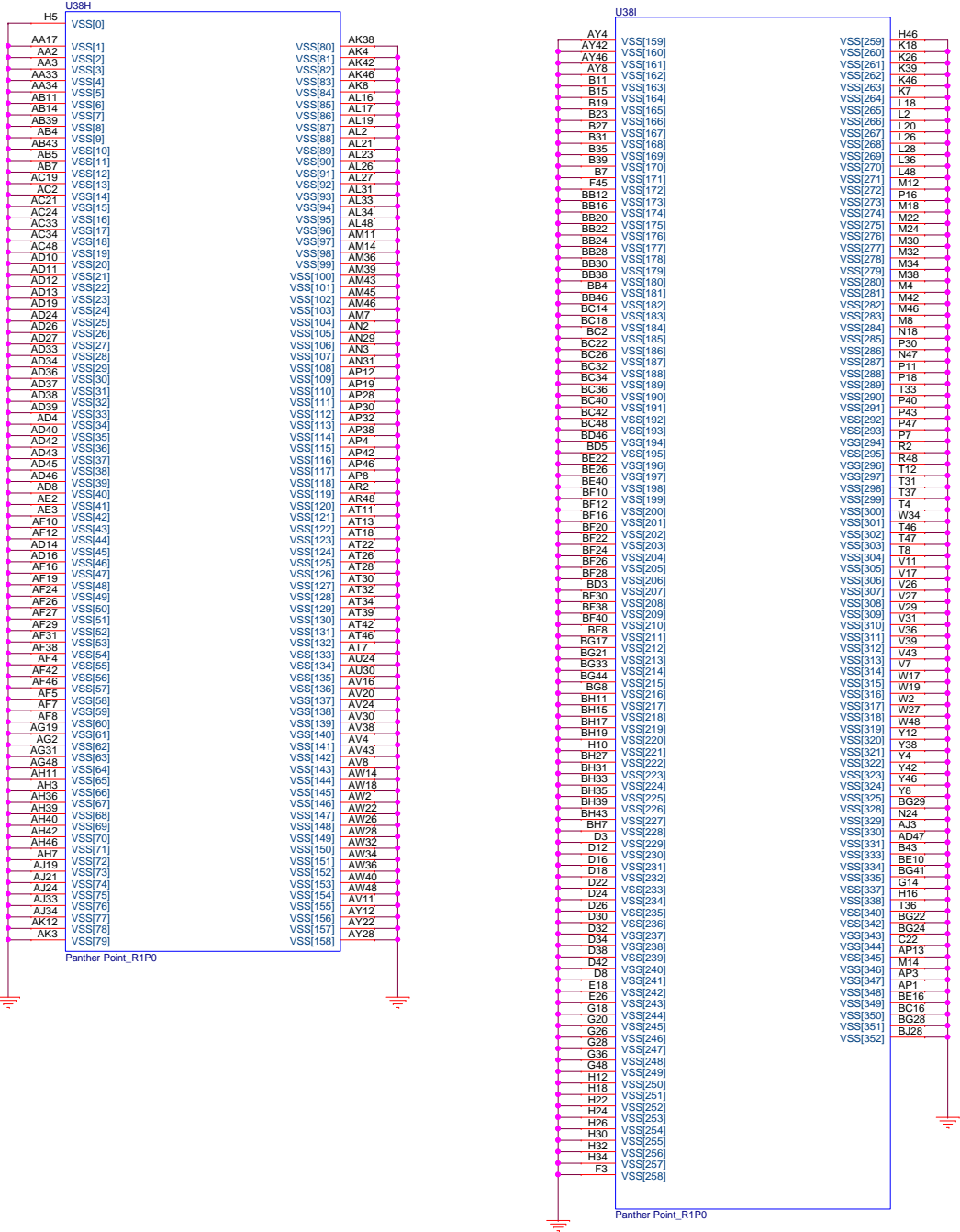
Reserve +3V\_S5 to VCCSPI for EC 795 co-layout



20111018 ADD DSW Cricuit  
20111030 modify cuirucit.

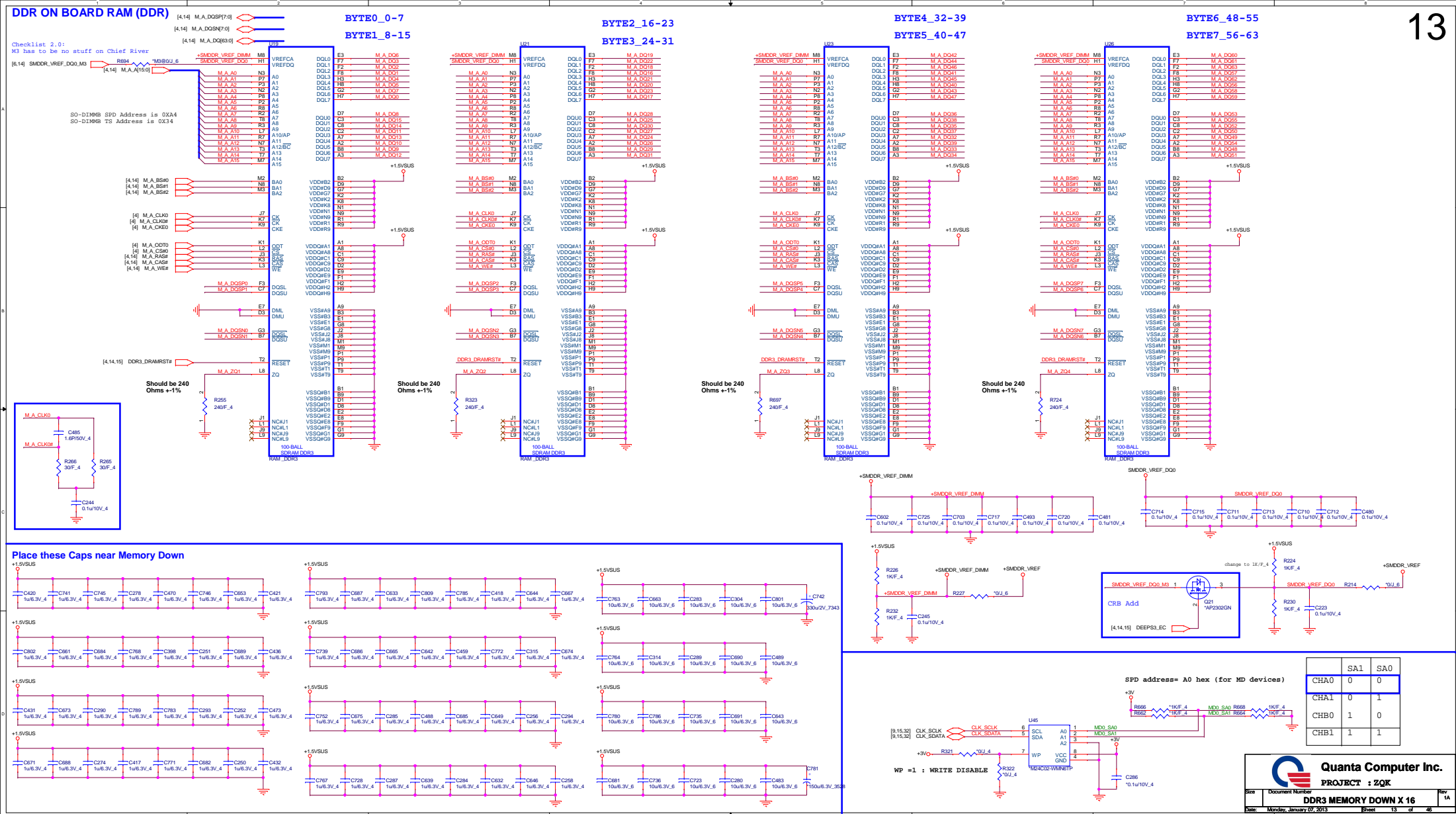


IBEX PEAK-M (GND) (CLG)



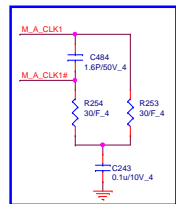
Quanta Computer Inc.  
PROJECT : ZQK







BYTE6_48-55	
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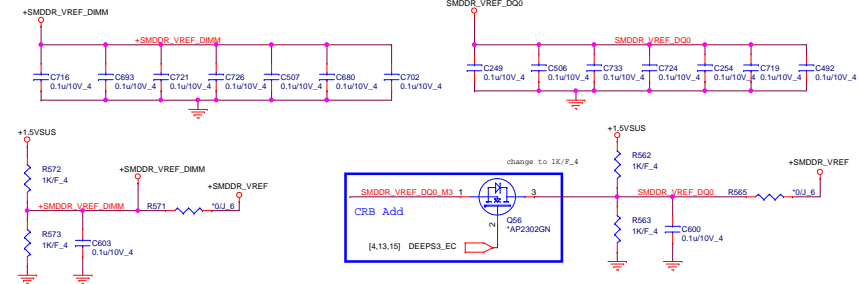
Should be 2  
Ohms  $\pm 1\%$



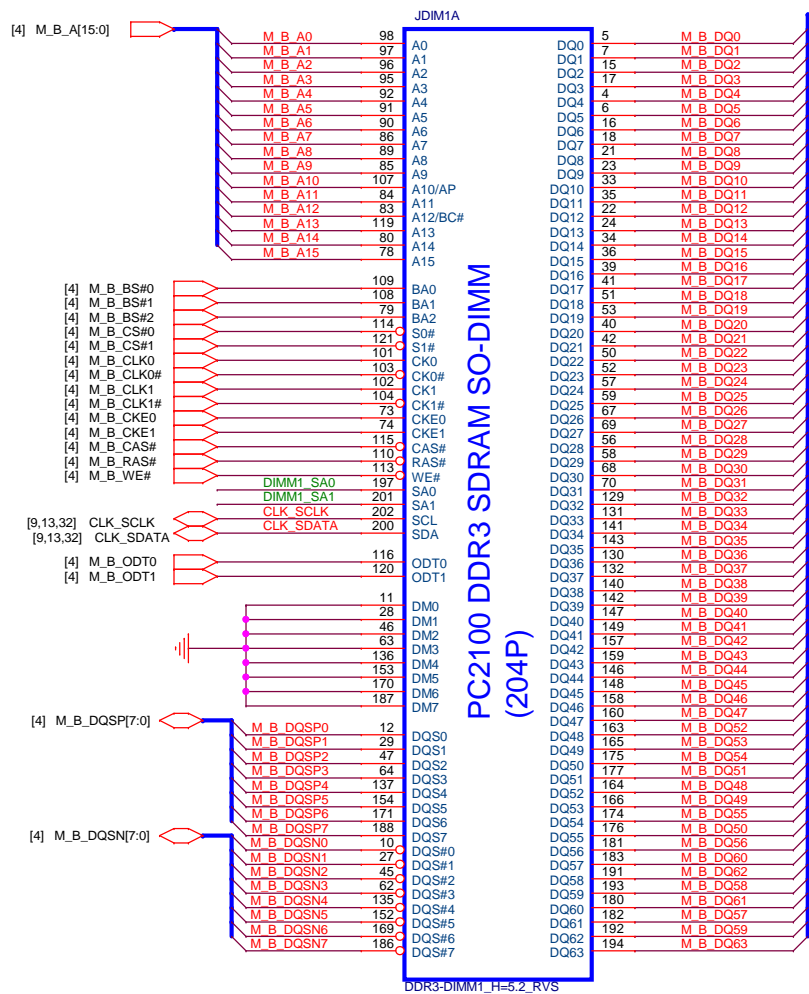
Should be 2  
Ohms  $\pm 1\%$



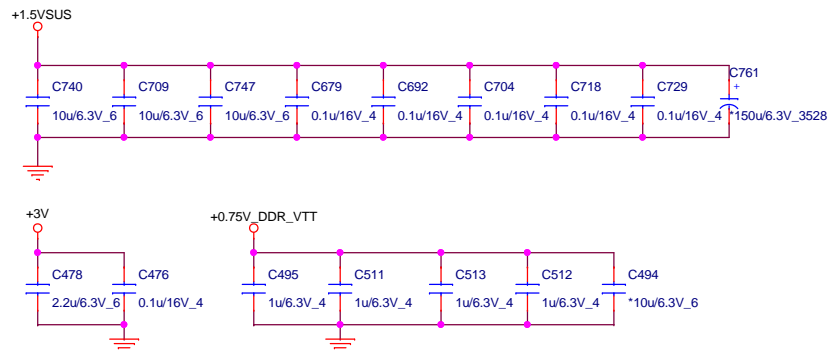
Should be 2  
Ohms  $\pm 1\%$



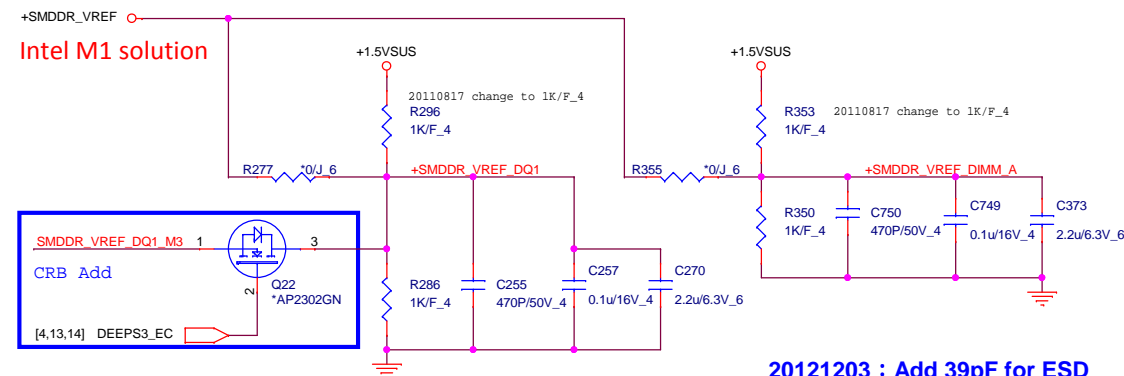




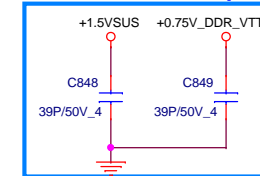
Place these Caps near SO\_DIMM-A



Intel M1 solution

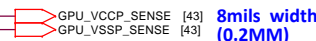



20121203 : Add 39pF for ESD



	SA1	SA0
CHA0	0	0
CHA1	0	1
CHB0	1	0
CHB1	1	1





 <b>Quanta Computer Inc.</b> <b>PROJECT : ZQK</b>		Rev 1A
Size	Document Number	
<b>DGPU 1/5 (PEG)</b>		
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Logical Strapping Bit	PU-VDD	PD
4.99K	1000	0000
10K	1001	0001
15K	1010	0010
20K	1011	0011
24.9K	1100	0100
30.1K	1101	0101
34.8K	1110	0110
45.3K	1111	0111

Logical Strapping Bit	Logical Strapping Bit	Logical Strapping Bit	Logical Strapping Bit
ROM_SO	FB_1	FB_0	SMB_ALT_ADDR
ROM_SCLK	PCI_DEV[4]	SUB_VENDOR	PCI_DEV[5]
ROM_S1	RAMCFG[3]	RAMCFG[2]	RAMCFG[1]
STRAP0	USER[3]	USER[2]	USER[1]
STRAP1	3GIO_PADCFG[3]	3GIO_PADCFG[2]	3GIO_PADCFG[1]
STRAP2	PCI_DEV[3]	PCI_DEV[2]	PCI_DEV[1]
STRAP3	SOR3_EXPOSED	SOR2_EXPOSED	SOR0_EXPOSED
STRAP4	RESERVED	PCI_SPEED_CHANGE_GEN3	PCI_MAX_SPEED

STRAP3	
Optimus	→ 4.99k PD
Discrete only	→ 15K PD

Resistor P/N	
4.99K	→ CS24992FB26
10K	→ CS31002FB26
15K	→ CS31502FB24
20K	→ CS32002FB29
24.9K	→ CS32492FB16
30.1K	→ CS33012FB18
34.8K	→ CS34822FB22
45.3K	→ CS34532FB18

Table 123 Binary Strap Mode Mapping

Strap Pin Name	Strap Mapping	Resistance	Polarity
ROM_SCLK	SMB_ALT_ADDR	10k Ω	Pull-down to GND
ROM_S1	SUB_VENDOR	10k Ω	Pull-up to 3V3 if VBIOS ROM exists Pull-down to GND if no VBIOS ROM
ROM_SO	VGA_DEVICE	10k Ω	Pull-down to GND (no display)
STRAP0	RAM_CFG[0]	10k Ω	See Note below
STRAP1	RAM_CFG[1]	10k Ω	See Note below
STRAP2	RAM_CFG[2]	10k Ω	See Note below
STRAP3	RAM_CFG[3]	10k Ω	See Note below
STRAP4	PCIE_MAX_SPEED	10k Ω	Pull-down to GND

N14M-GE device ID is 0x1140  
N14M-GE is use binary strap setting

A.ROM\_S1 - 10k pull down  
B.ROM\_SO - 10k pull down  
F.STRAP 3 - 10k pull down

Micron: MT41K256M16HA-107G:E (QPN = AKD5PGSTL05)  
strap = 0x0 = (0x101)  
STRAP 3&2&0 = 10K Pull high  
STRAP 1 = 10K Pull down

A.ROM\_S1 - Memory strap

B.ROM\_SO - 5k pull high

D.STRAP 0 - 45k pull high

E.STRAP 1 - GV2 - 45k pull down

F.STRAP 3 - 5k pull down

C2.For N14P-GV2+SDR3 sku

N14P-GV2 OS device ID=0x1292 'This is QS device ID

1.ROM\_SCLK=5K pull high

2.STRAP2=15k pull down

3.STRAP4=45k pull down For N14P-GV2 QS

N14P-GT device ID=0x0FE4

1.ROM\_SCLK=15K pull down

2.STRAP2=25k pull down

5.STRAP4=45k pull down

Table 3. N14M-G5/LP and N14P-GV2 DDR3 Recommended Memories 128Mx16 Configuration

Configuration	Vendor	Strap	FBVDD/ FBVDDQ	Manufacturer Part Number	Max Speed (MHz)	Memory Date Code Minimum	Status
128Mx16 DDR3	Samsung	0x7	1.5 V/ 1.5 V	K4V2G1646E-BC1A	1000	1204	Production Candidate
			1.5 V/ 1.5 V	K4V2G1646E-BC11	900	1204	Production Candidate
	Micron	0x5	1.5 V/ 1.5 V	AT41J128M16JT-093G-K	1000	1150	Production Candidate
			1.5 V/ 1.5 V	AT41J128M16JT-107G-K	900	1150	Production Candidate
256Mx16 DDR3	Samsung	0x3	1.5 V/ 1.5 V	K4V4G1646E-BC11	900	H/A	Production Candidate
			1.5 V/ 1.5 V	AT41K256M16HA-107G-E	900	H/A	Production Candidate
	Micron	0x1	1.5 V/ 1.5 V	AT41K256M16HA-107G-E	900	H/A	Production Candidate
			1.5 V/ 1.5 V	HSTQ4G32FR-11C	900	H/A	Production Candidate

Table 8. N14P-G5/LP/GE/GT DDR3 Recommended Memories 128Mx16 Configuration

Configuration	Vendor	Strap	FBVDD/ FBVDDQ	Manufacturer Part Number	Max Speed (MHz)	Memory Date Code Minimum	Status
128Mx16 DDR3	Samsung	0x7	1.5 V/ 1.5 V	K4V2G1646E-BC1A	1000	1204	Production ready
			1.5 V/ 1.5 V	K4V2G1646E-BC11	900	1204	Production ready
	Micron	0x5	1.5 V/ 1.5 V	AT41J128M16JT-093G-K	1000	1234	Production ready
			1.5 V/ 1.5 V	AT41J128M16JT-107G-K	900	1234	Production ready
256Mx16 DDR3	Samsung	0x3	1.5 V/ 1.5 V	K4V4G1646E-BC1A	1000	1204	Production ready
			1.5 V/ 1.5 V	AT41K256M16HA-107G-E	900	1204	Production ready
	Micron	0x1	1.5 V/ 1.5 V	AT41K256M16HA-107G-E	900	H/A	Production ready
			1.5 V/ 1.5 V	HSTQ2G63FR-11C	900	H/A	Production ready

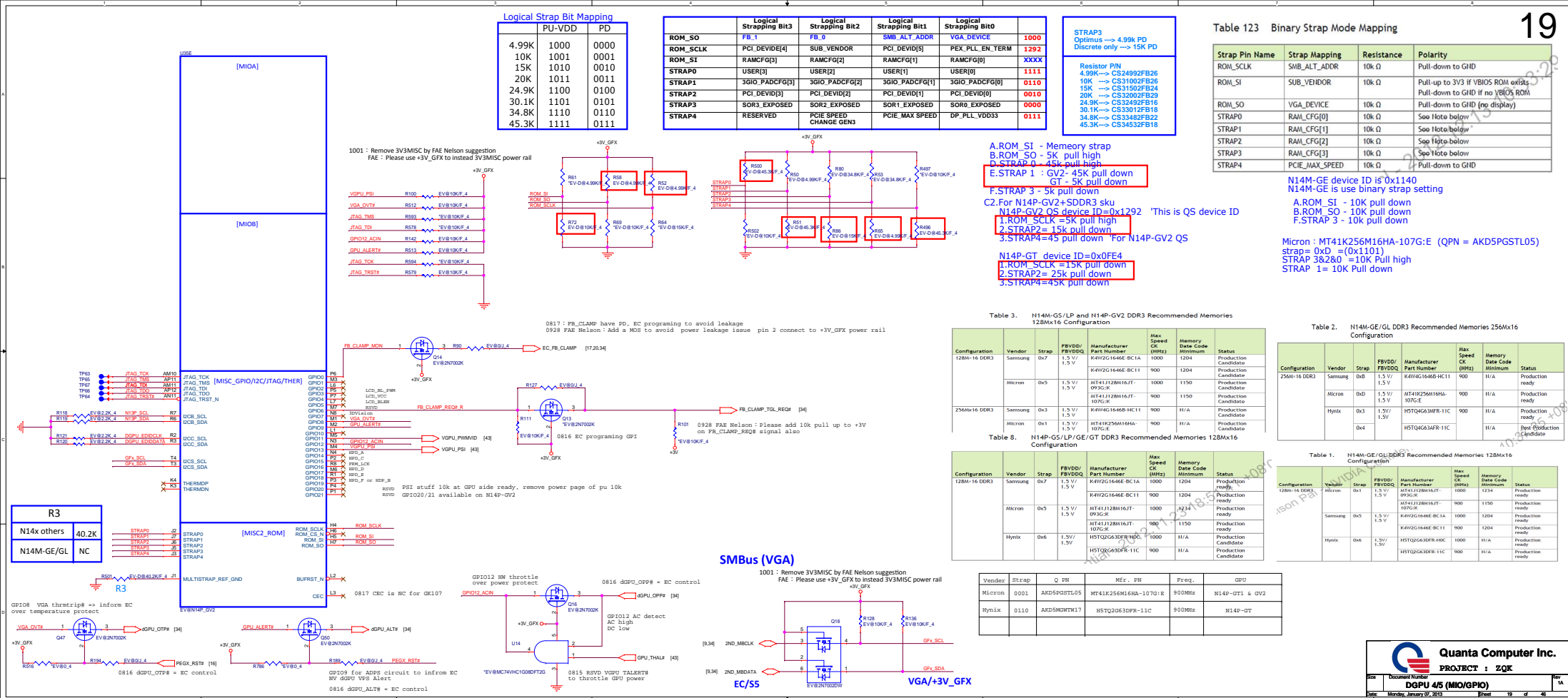
Table 2. N14M-GE/GL DDR3 Recommended Memories 256Mx16 Configuration

Configuration	Vendor	Strap	FBVDD/ FBVDDQ	Manufacturer Part Number	Max Speed (MHz)	Memory Date Code Minimum	Status
256Mx16 DDR3	Samsung	0x5	1.5 V/ 1.5 V	K4V4G1646E-BC11	900	H/A	Production ready
			1.5 V/ 1.5 V	AT41K256M16HA-107G-E	900	H/A	Production ready
	Micron	0x5	1.5 V/ 1.5 V	AT41K256M16HA-107G-E	900	H/A	Production ready
			1.5 V/ 1.5 V	HSTQ4G32FR-11C	900	H/A	Production ready

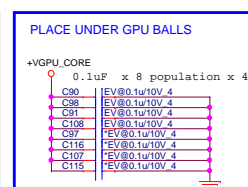
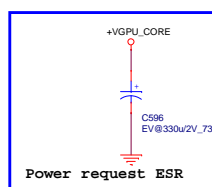
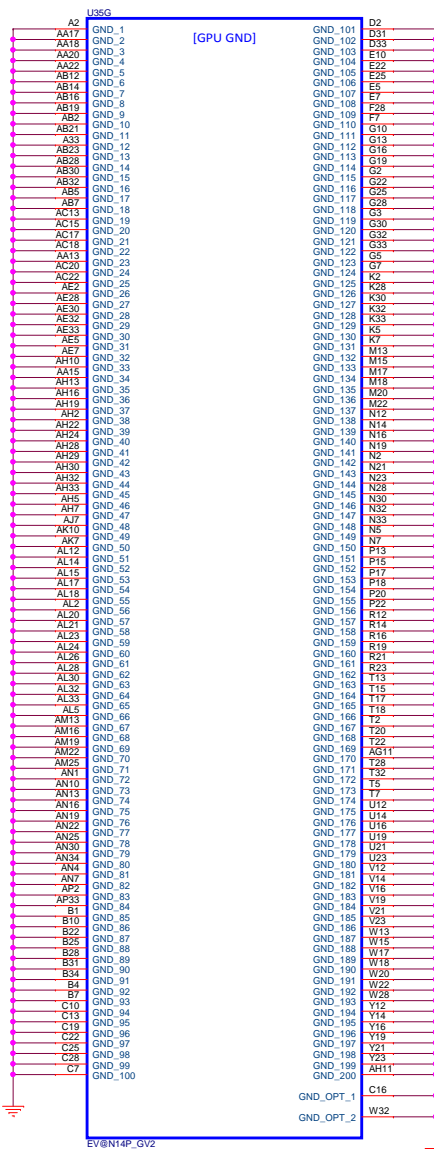
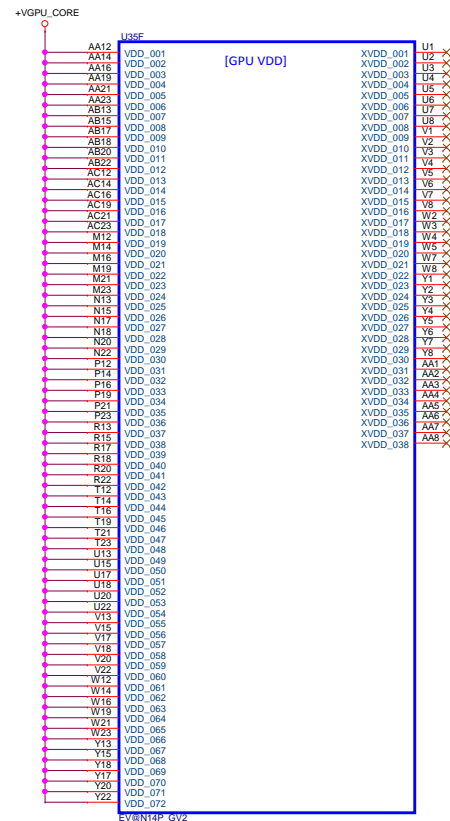
Table 1. N14M-GE/GL DDR3 Recommended Memories 128Mx16 Configuration

Configuration	Vendor	Strap	FBVDD/ FBVDDQ	Manufacturer Part Number	Max Speed (MHz)	Memory Date Code Minimum	Status
128Mx16 DDR3	Micron	0x1	1.5 V/ 1.5 V	AT41J128M16JT-093G-K	1000	1234	Production ready
			1.5 V/ 1.5 V	AT41J128M16JT-107G-K	900	1150	Production ready
	Samsung	0x5	1.5 V/ 1.5 V	K4V2G1646E-BC1A	1000	1204	Production ready
			1.5 V/ 1.5 V	K4V2G1646E-BC11	900	1204	Production ready

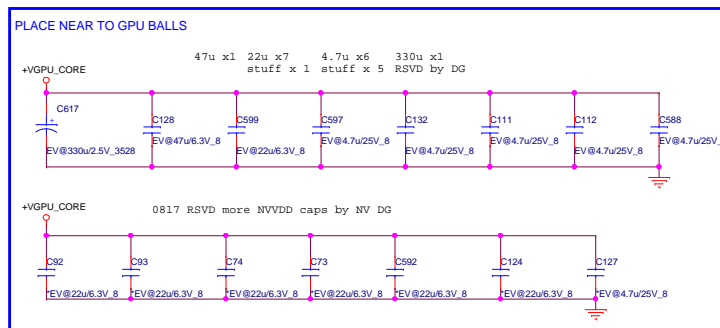
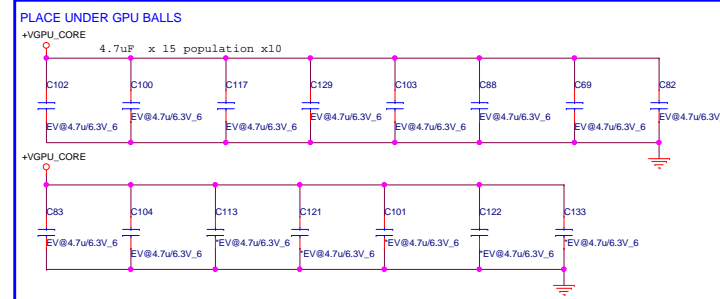
Vendor	Strap	Q PN	Ref. PN	Freq.	GPU
Micron	0001	AKD5PGSTL05	MT41K256M16HA-107G:E	900MHz	N14P-GT1 & GV2
Bynlix	0110	AKD5MGTW17	HSTQ2G63FR-11C	900MHz	N14P-GT



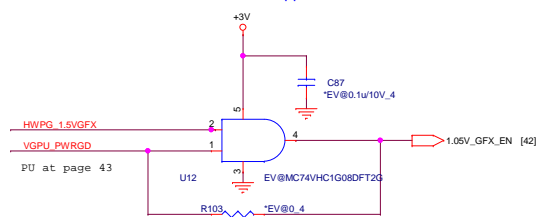
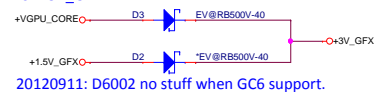




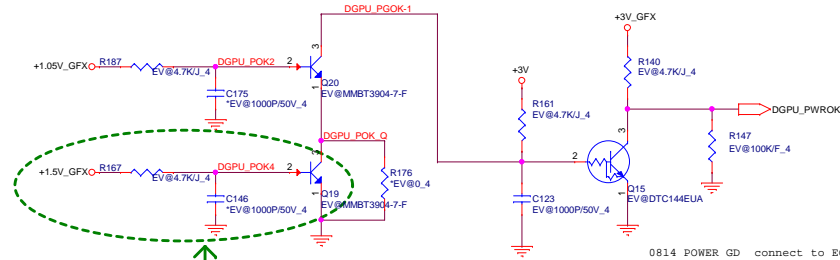
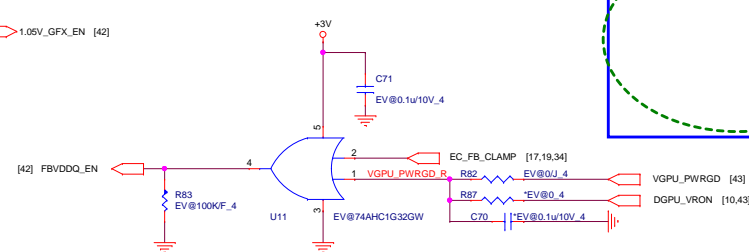
**LAYOUT NOTES:**  
UNDAER: WITHIN 150MILS  
NEAR: WITHIN 1378MILS



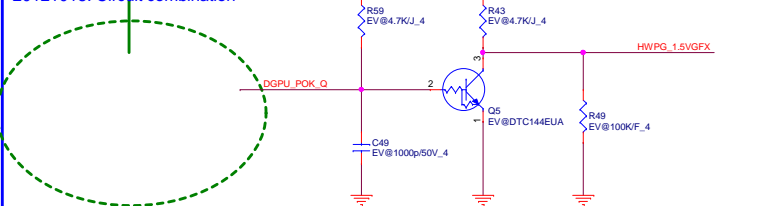
for meet Power down sequence  
for +3V GFX



0816 GC6 need system 3V to control FBVDDQ

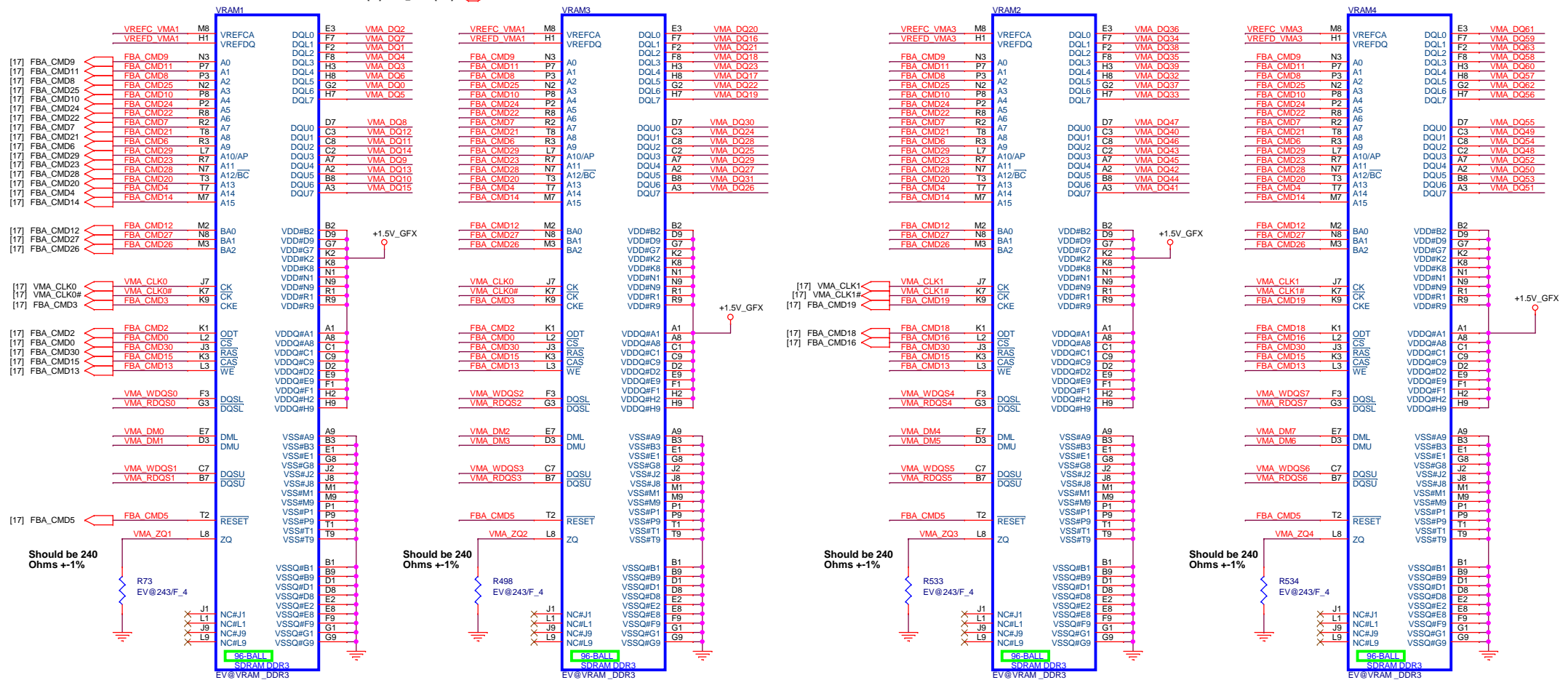


20120914: H/W Add for HWPG\_1.5VGFX  
2012018: Circuit combination



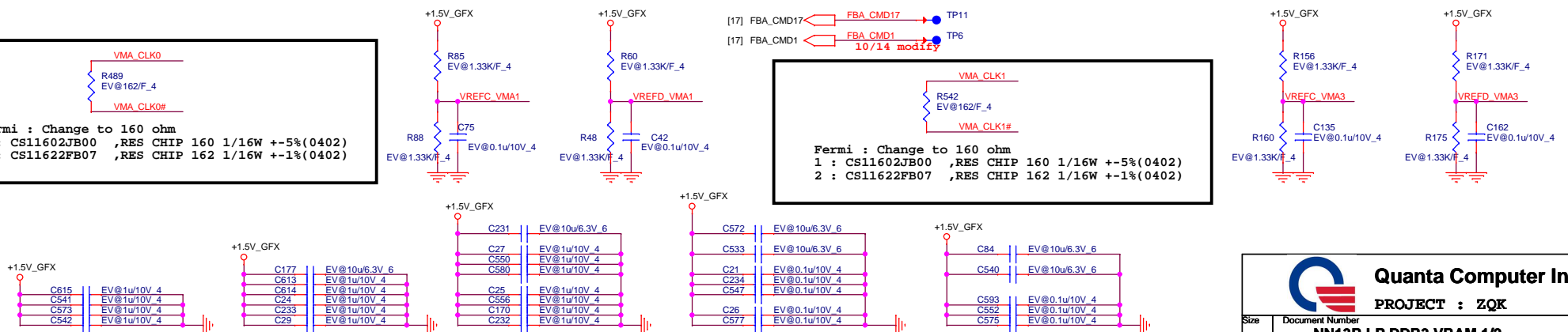


## CHANNEL A: 1024MB DDR3



```
Fermi : Change to 160 ohm
1 : CS11602JB00 ,RES CHIP 160 1/16W +-5%(0402)
2 : CS11622FB07 ,RES CHIP 162 1/16W +-1%(0402)
```

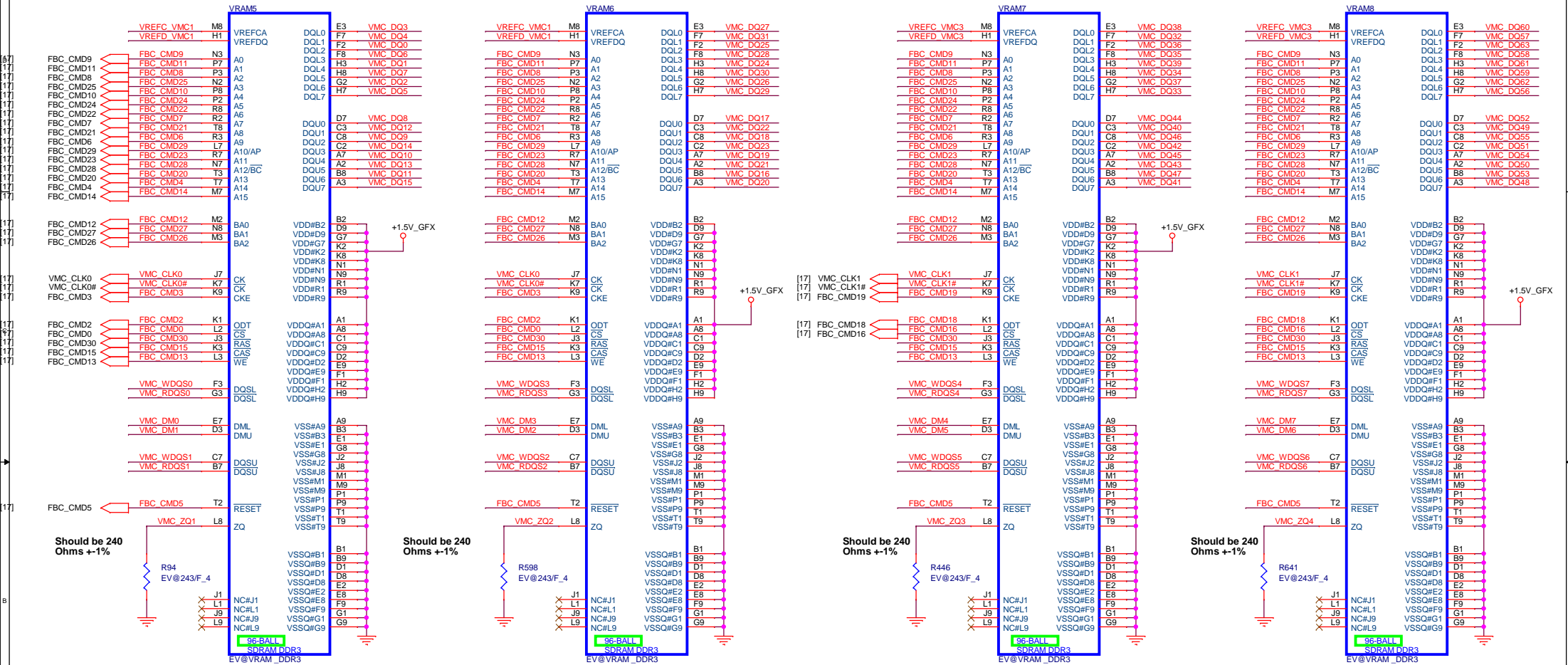
```
Fermi : Change to 160 ohm
1 : CS11602JB00 ,RES CHIP 160 1/16W +-5%(0402)
2 : CS11622FB07 ,RES CHIP 162 1/16W +-1%(0402)
```





[17] VMC\_DQ[63..0]  
[17] VMC\_DM[7..0]  
[17] VMC\_WDQS[7..0]  
[17] VMC\_RDQS[7..0]

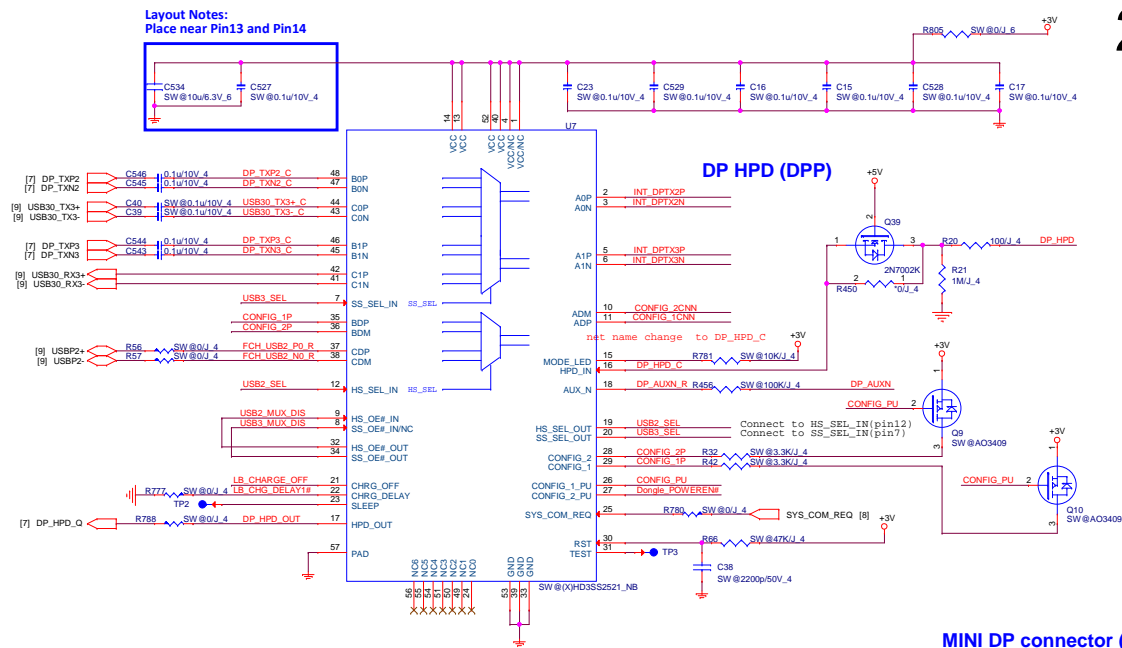
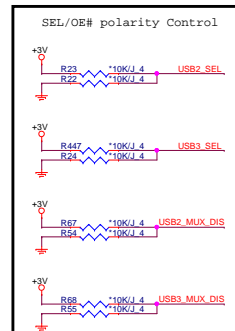
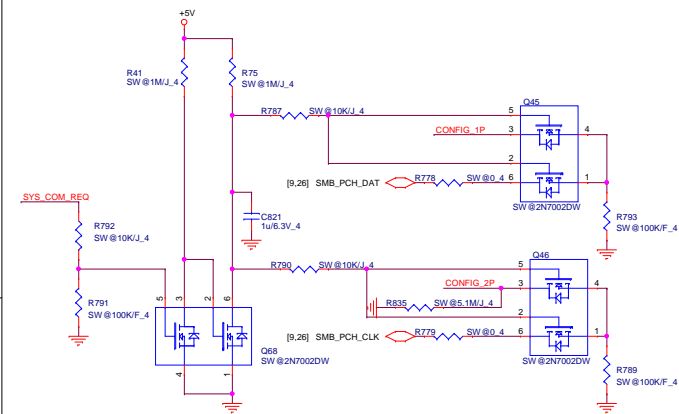
## CHANNEL B: 1024MB DDR3



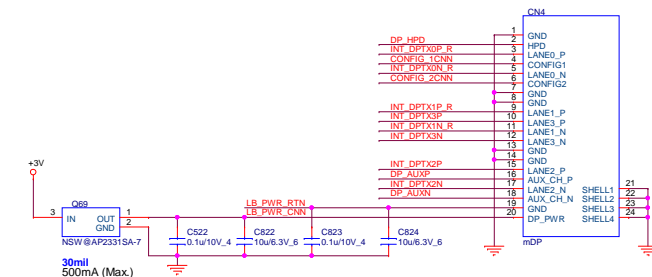
Fermi : Change to 160 ohm  
 1 : CS11602JB00 ,RES CHIP 160 1/16W +-5%(0402)  
 2 : CS11622FB07 ,RES CHIP 162 1/16W +-1%(0402)

Fermi : Change to 160 ohm  
 1 : CS11602JB00 ,RES CHIP 160 1/16W +-5%(0402)  
 2 : CS11622FB07 ,RES CHIP 162 1/16W +-1%(0402)

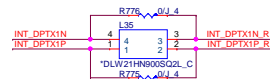
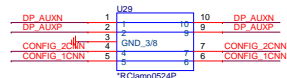
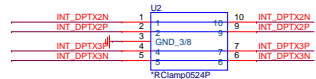




### MINI DP connector (DPP)



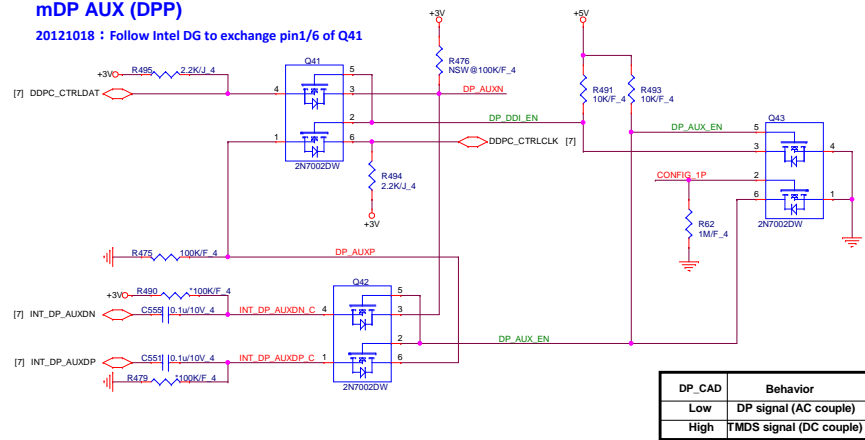
## ESD Protect (EMC)



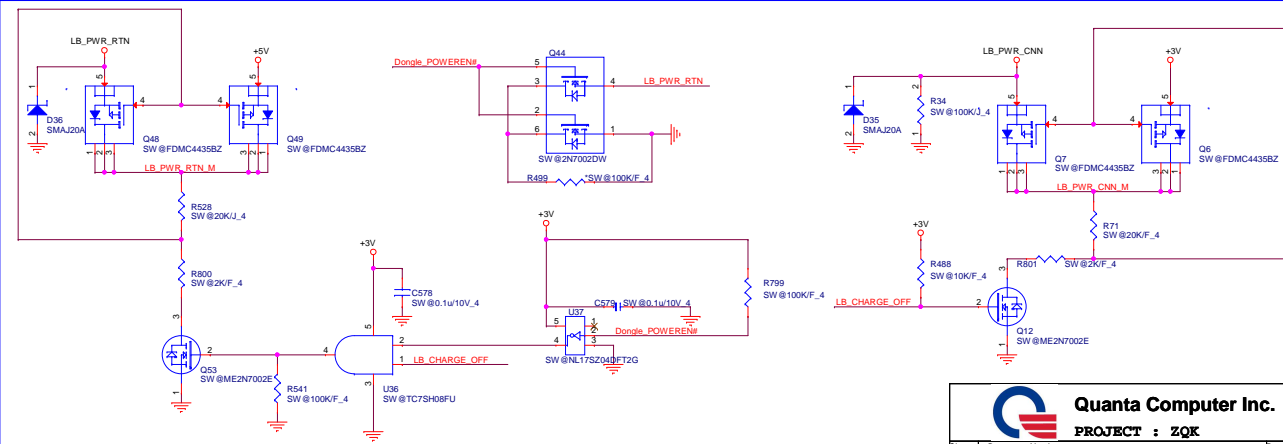
**Layout Notes:**  
Place decoupling CAPs close to Connector

mDP AUX (DPP)

**20121018 : Follow Intel DG to exchange pin1/6 of Q41**

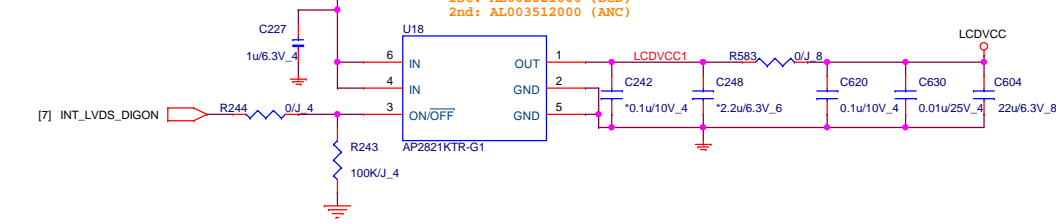


DP_CAD	Behavior
Low	DP signal (AC couple)
High	TMDS signal (DC couple)

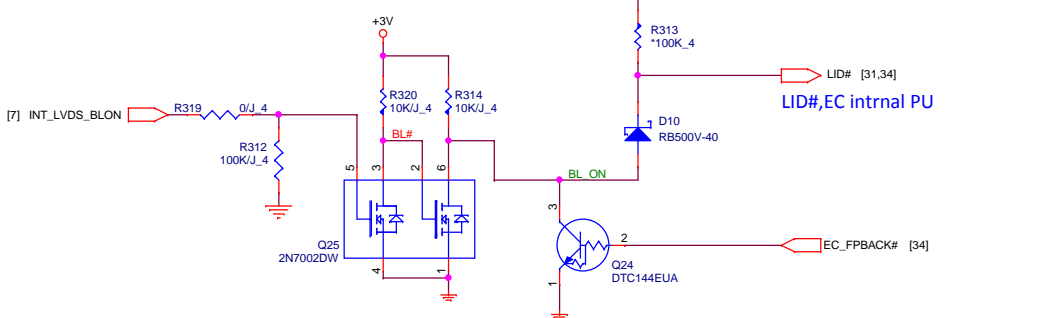




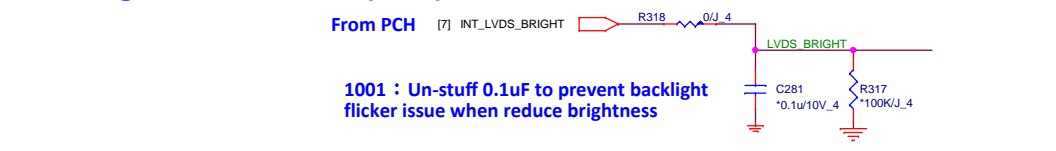
# eDP Power (LDS)



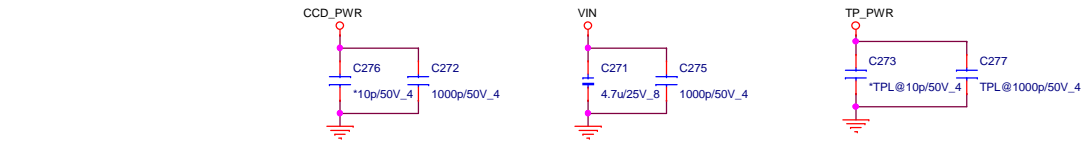
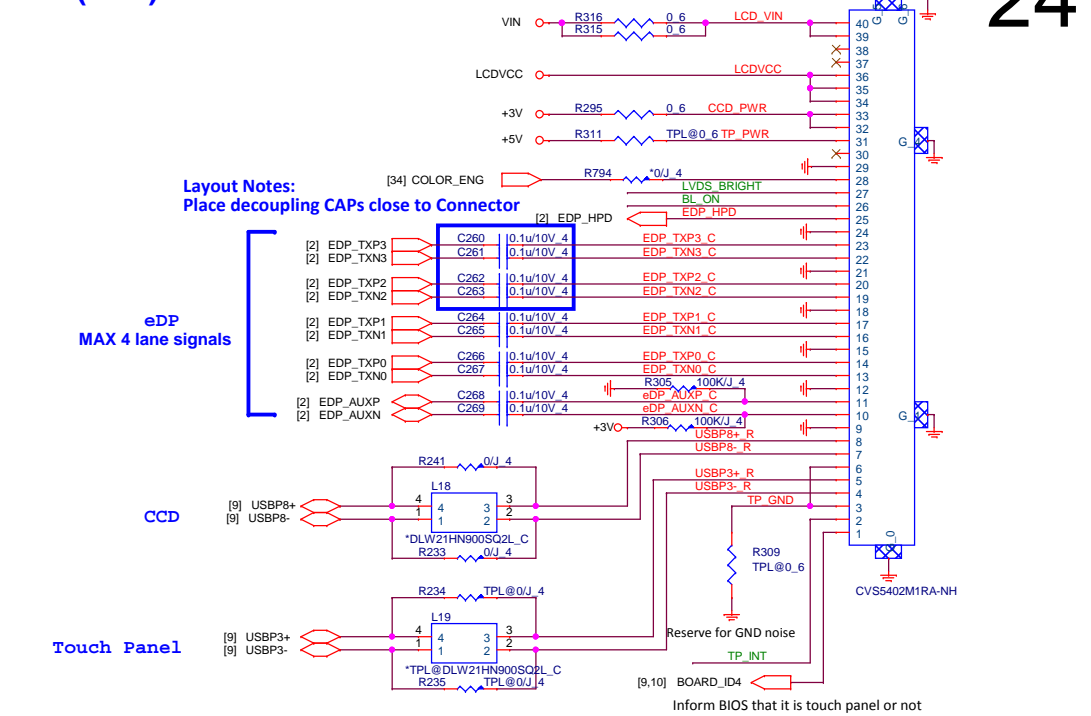
# eDP Backlight Control (LDS)



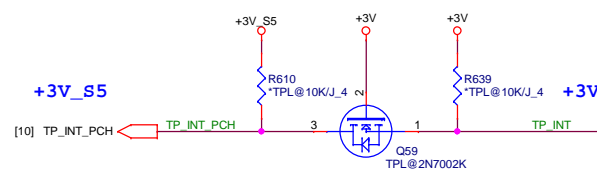
# eDP Brightness Control (LDS)



# eDP (LDS)

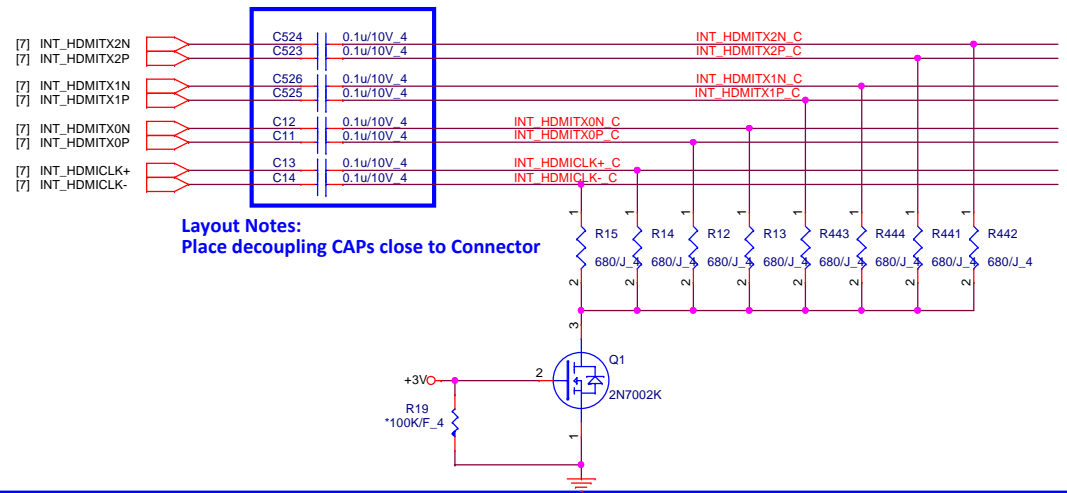


Touch Panel interrupt signal :  
1016 : Exchange Q59 pin 1 & 3 direction to prevent leakage

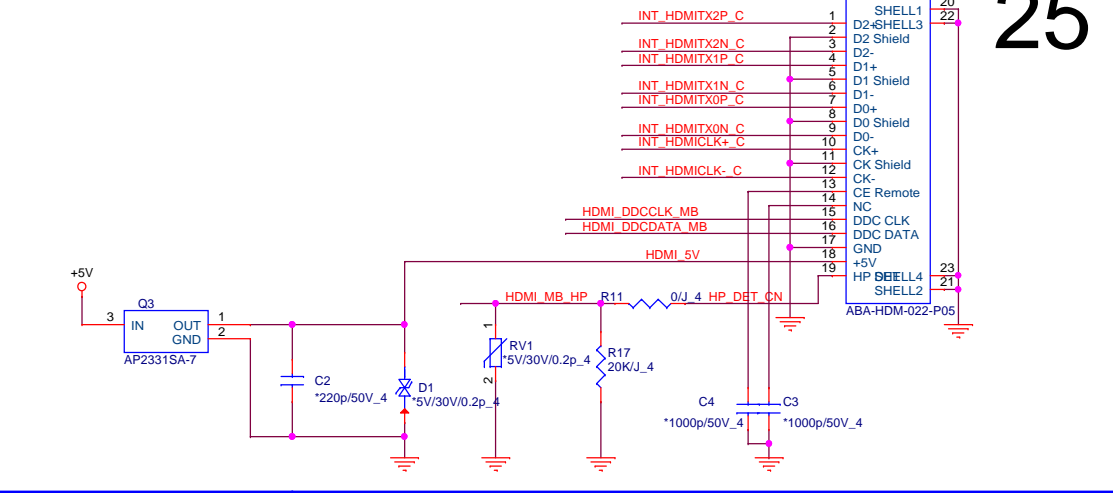




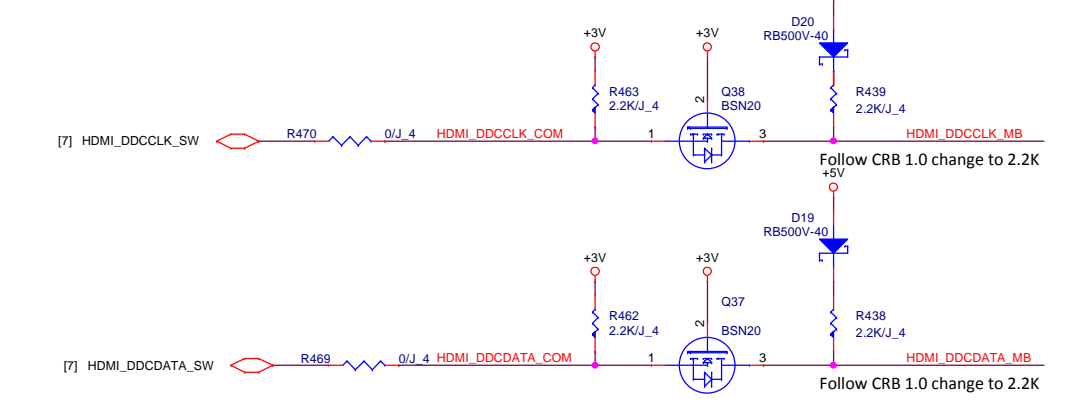
## HDMI Cost Reduced level shift (HDM)



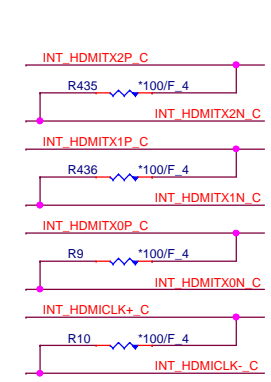
## HDMI connector (HDM)



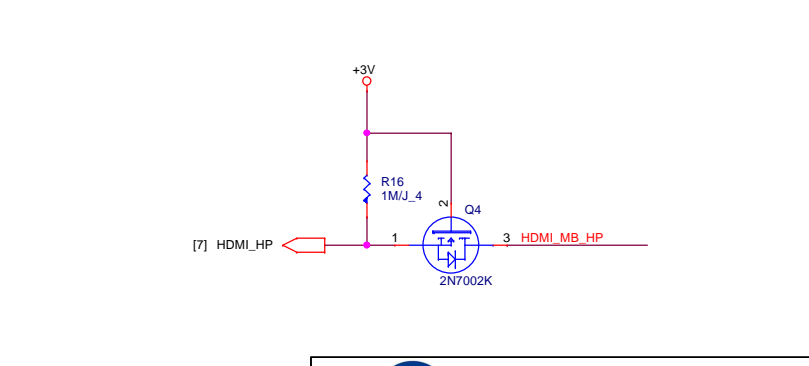
## HDMI DDC (HDM)




## EMI (EMC)



## HDMI-detect (HDM)



**Quanta Computer Inc.**

PROJECT : ZQK

Size

Document Number

HDMI

Rev  
1A

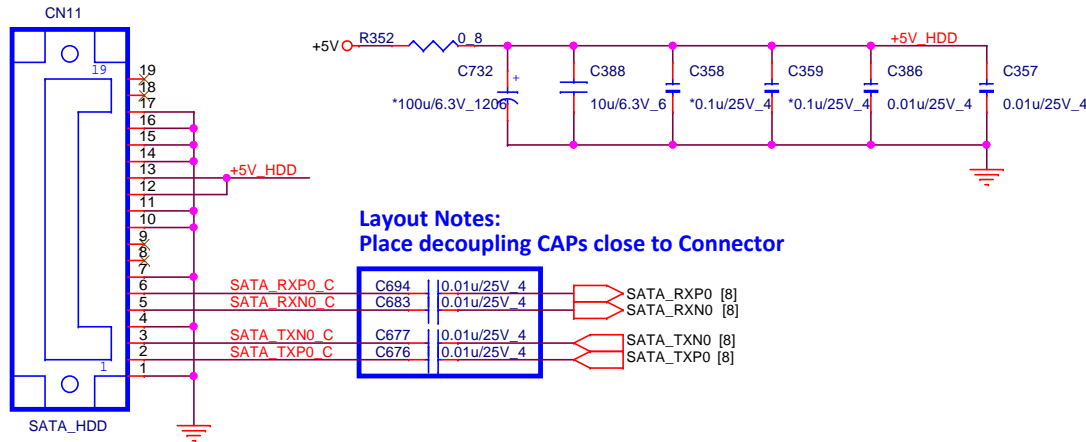
Date: Monday, January 07, 2013Sheet 25 of 46





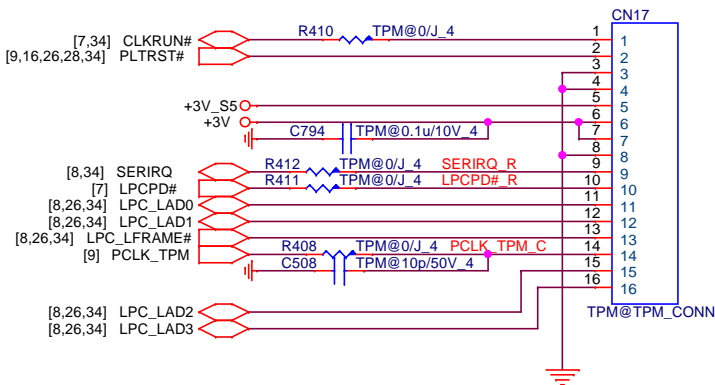


MAIN SATA HDD (HDD)

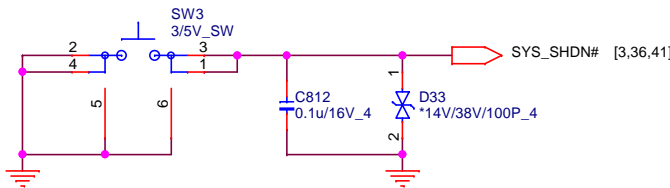


TPM (TPM)

27



3/5VPCU reset switch (CLG)







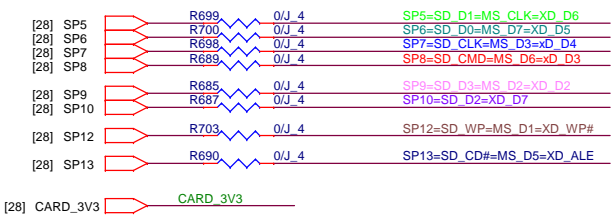
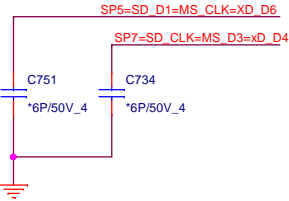


CARD READER CONNECTOR (MMC)

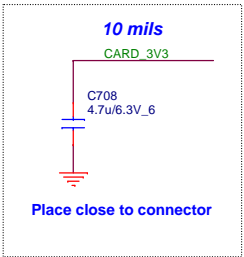
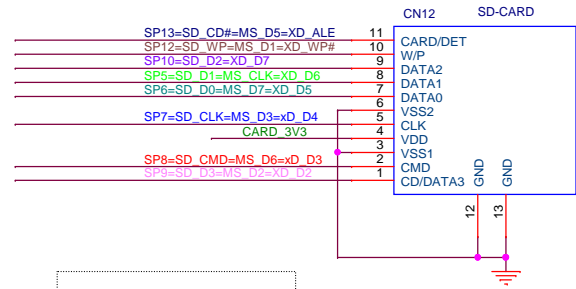
Share Pin

SP1	SD D7			xD RDY
SP2	SD D6	MS INS#		xD RE#
SP3	SD D5			xD CE#
SP4	SD D4			xD WE#
SP5	SD D1	MS CLK		xD D6
SP6	SD D0	MS D7		xD D5
SP7	SD CLK	MS D3		xD D4
SP8	SD CMD	MS D6		xD D3
SP9	SD D3	MS D2		xD D2
SP10	SD D2			xD D7
SP11		MS BS		xD CLE
SP12	SD WP	MS D1		xD WP#
SP13	SD CD#	MS D5		xD ALE
SP14		MS D4		xD D0
SP15		MS D0		xD D1
SP16				xD CD#

EMI

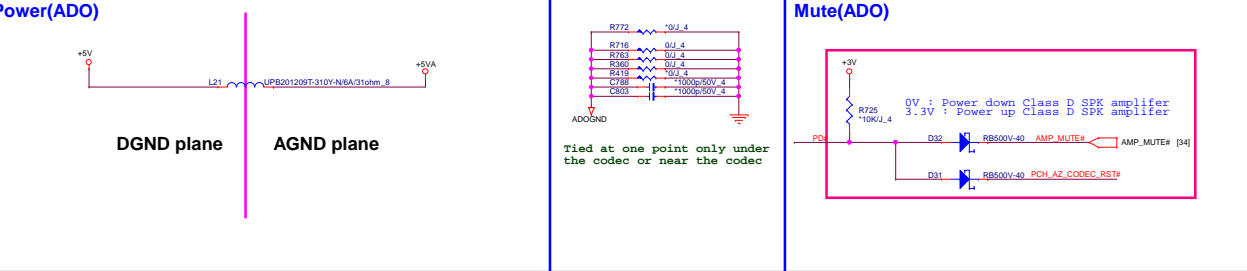
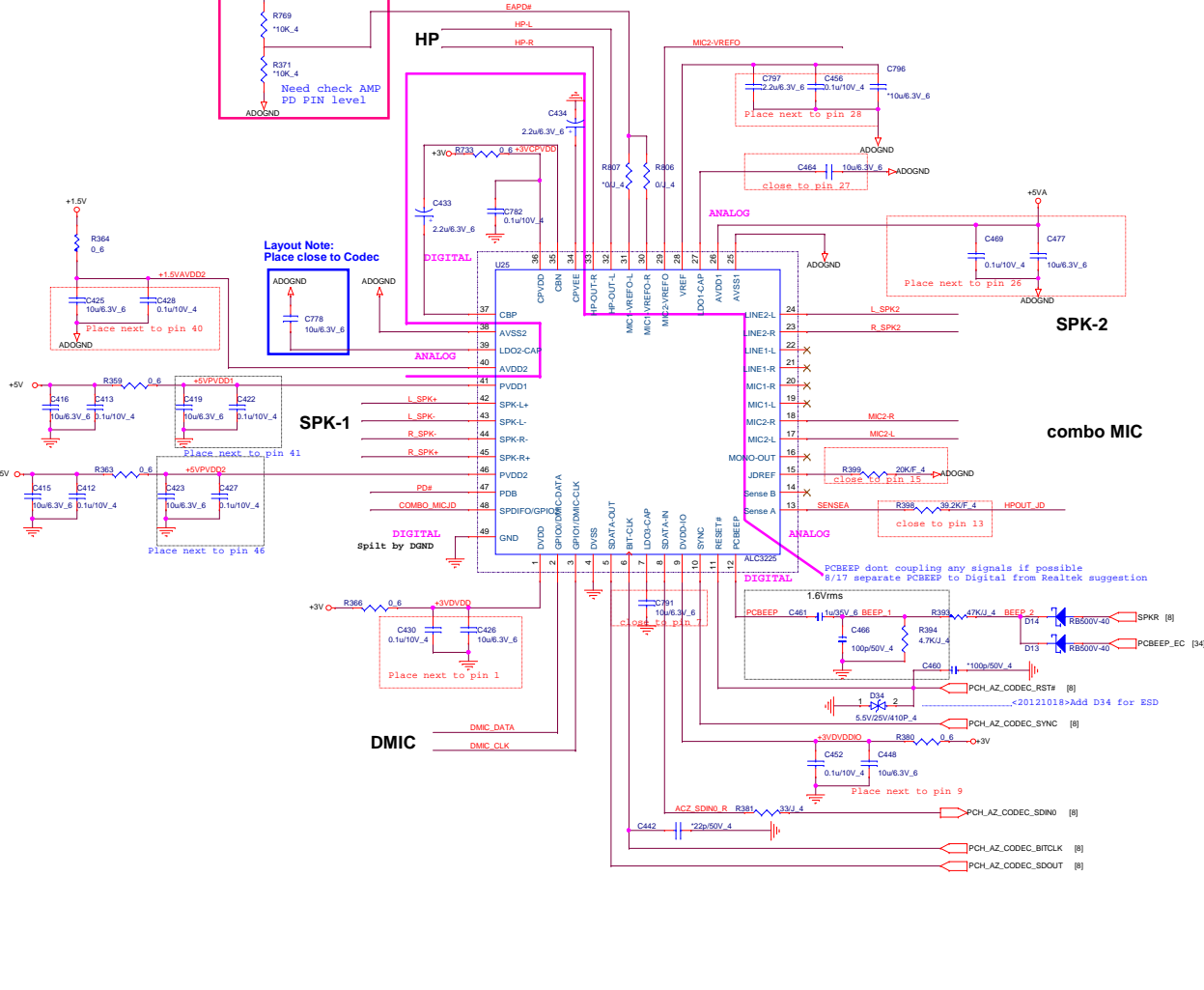


SD/MMC CARD READER (MMC)

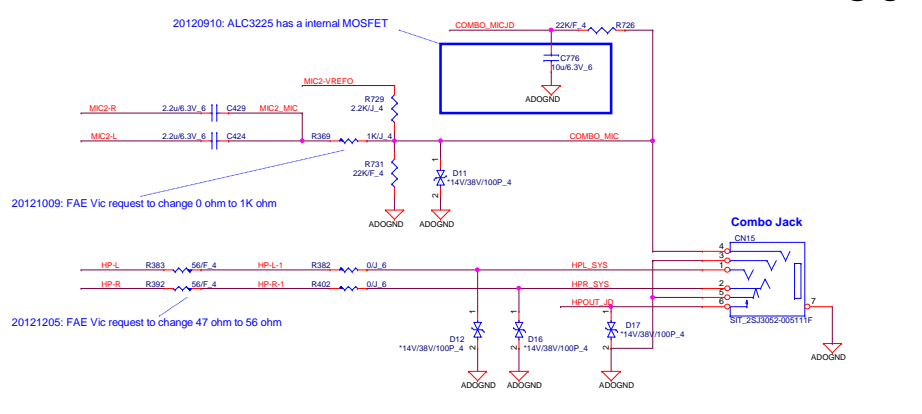




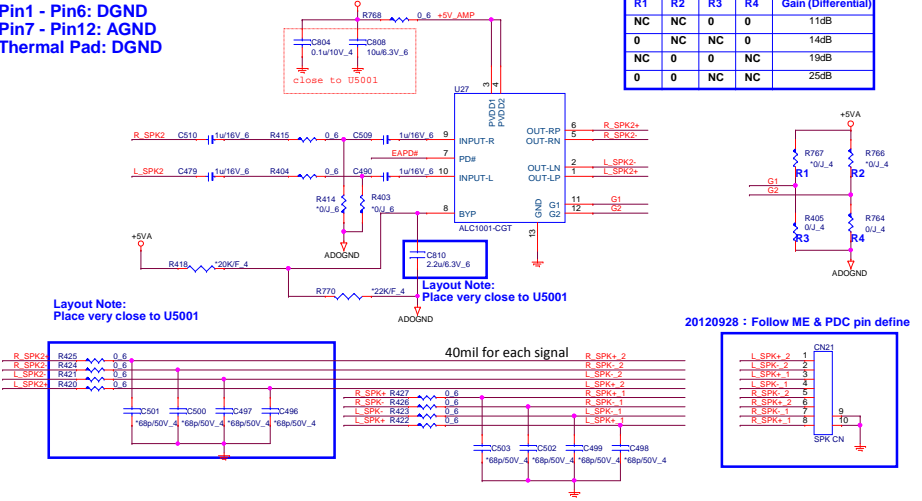
Codec (ADO)



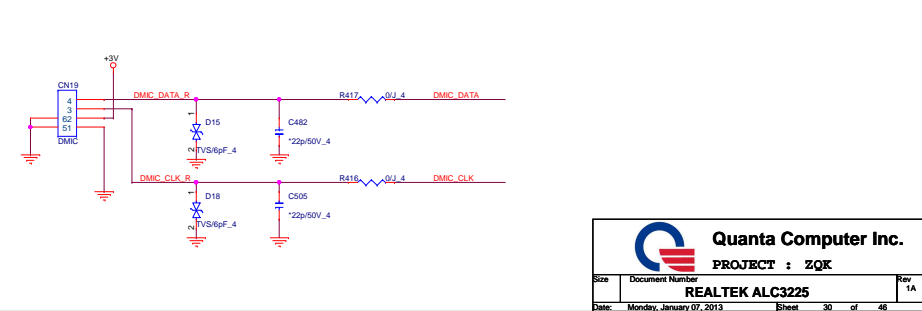
HEADPHONE/Mic combo (AMP)



Internal Speaker (AMP)



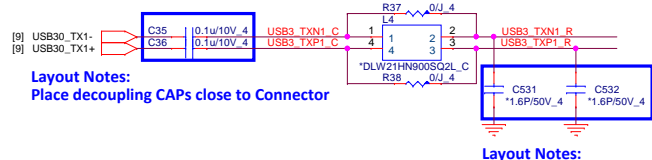
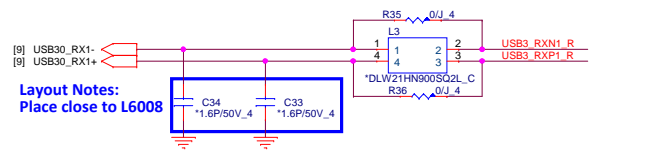
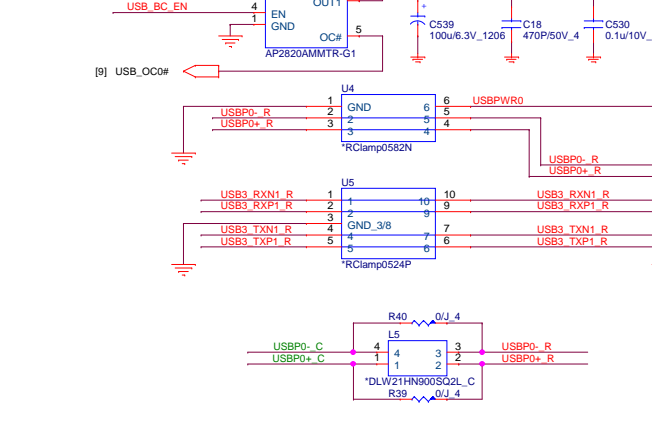
INT DMIC (AMP)





# USB3.0 (USB)

2012-06-15  
Active High:  
1st: AL002820003 (BCD)  
2nd: AL007534001 (Promate)  
3rd: AL002511002 (DDS)



**Layout Notes:**  
Place close to L6008

**Layout Notes:**  
Place decoupling CAPs close to Connector

**Layout Notes:**  
Place close to L6009

**Layout Notes:**  
Place close to L6009

**Layout Notes:**  
Place close to L6009

**Layout Notes:**  
Place close to L6009

**Layout Notes:**  
Place close to L6009

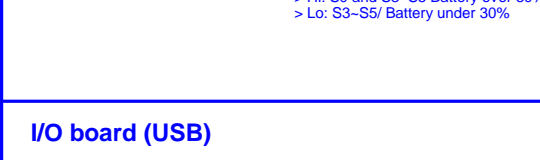
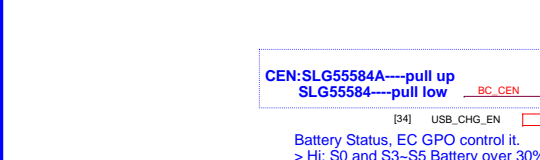
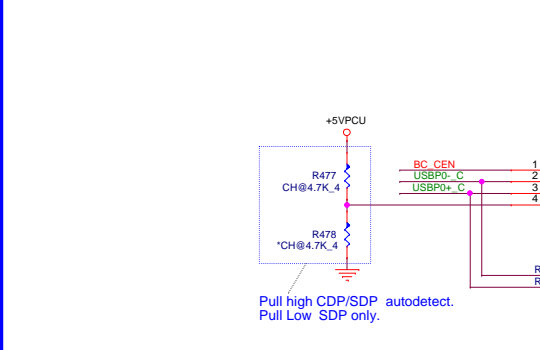
**Layout Notes:**  
Place close to L6009

**Layout Notes:**  
Place close to L6009

# USB Charger to 3.0 (USB)

Name	USB data	State	Max Current	Apple Device
SDP	YES	S0-S3	500mA	500mA
CDP	YES	S0-S3	1500mA	500mA
DCP,Auto	NO	S4-S5	1800mA	1800mA

CH@: Default stuff



**Layout Notes:**  
Place close to L6008

**Layout Notes:**  
Place decoupling CAPs close to Connector

**Layout Notes:**  
Place close to L6009

**Layout Notes:**  
Place close to L6009

**Layout Notes:**  
Place close to L6009

**Layout Notes:**  
Place close to L6009

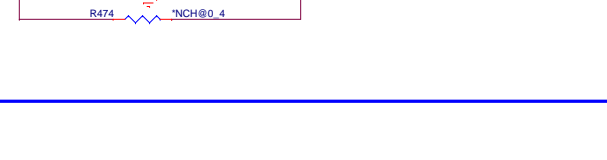
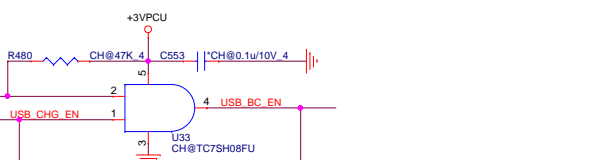
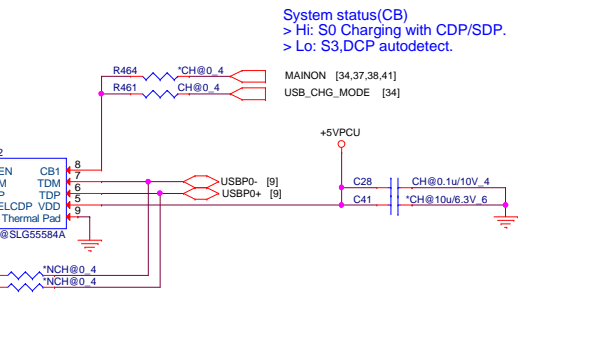
**Layout Notes:**  
Place close to L6009

**Layout Notes:**  
Place close to L6009

**Layout Notes:**  
Place close to L6009

CB	SELCDP	Function
0	X	DCP autodetect with mouse/keyboard wakeup
1	0	S0 charging with SDP only
1	1	S0 charging with CDP or SDP only (depending on external device)

CH@: Default stuff



**Layout Notes:**  
Place close to L6008

**Layout Notes:**  
Place decoupling CAPs close to Connector

**Layout Notes:**  
Place close to L6009

**Layout Notes:**  
Place close to L6009

**Layout Notes:**  
Place close to L6009

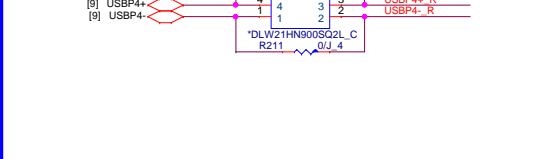
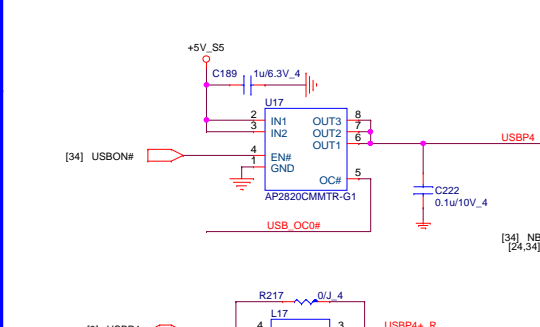
**Layout Notes:**  
Place close to L6009

**Layout Notes:**  
Place close to L6009

**Layout Notes:**  
Place close to L6009

**Layout Notes:**  
Place close to L6009

# I/O board (USB)

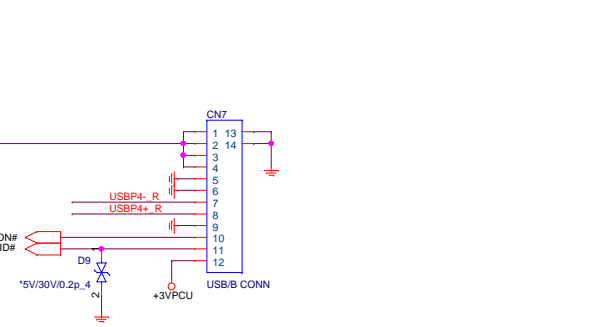


**Layout Notes:**  
Place close to L6008

**Layout Notes:**  
Place decoupling CAPs close to Connector

**Layout Notes:**  
Place close to L6009

# I/O board (USB)



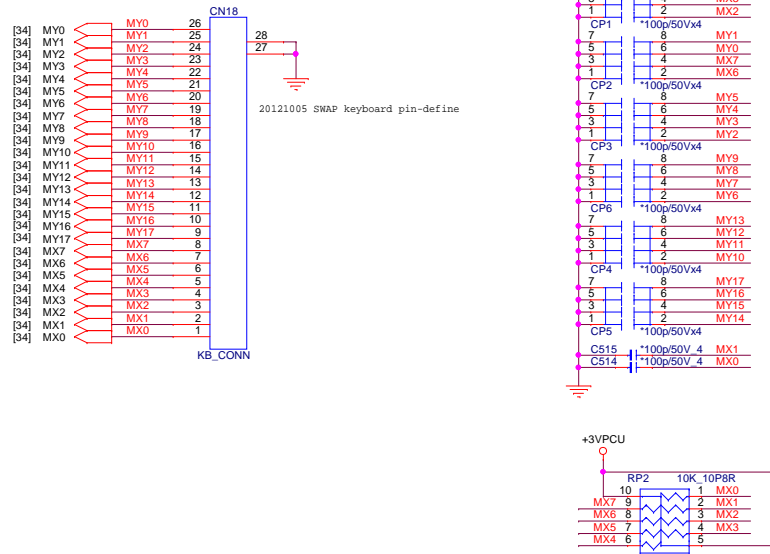
**Layout Notes:**  
Place close to L6008

**Layout Notes:**  
Place decoupling CAPs close to Connector

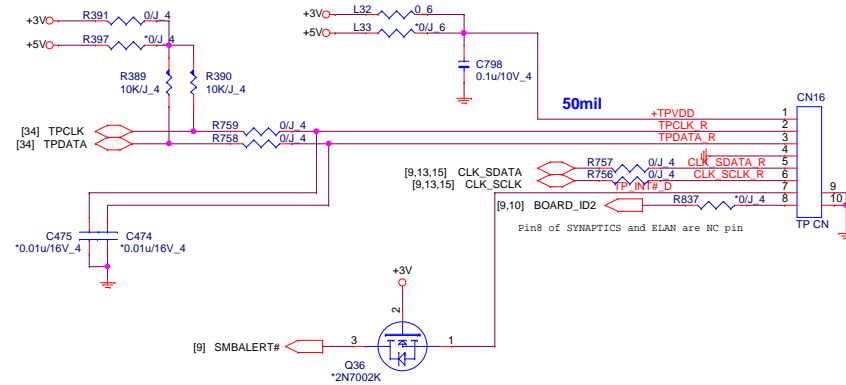
**Layout Notes:**  
Place close to L6009



## K/B (KBC)

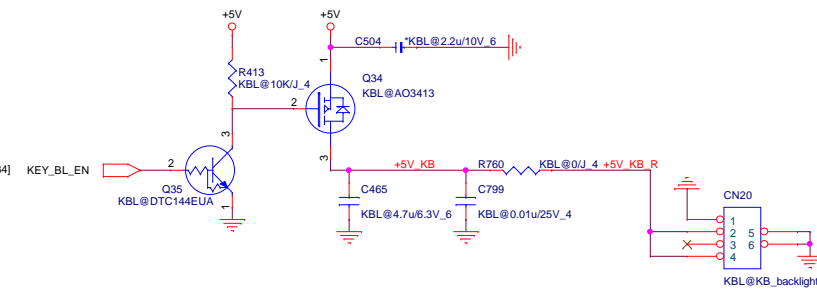


## TOUCHPAD BOARD CONN (TPD)

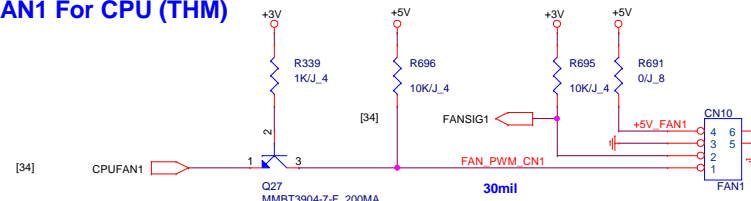


32

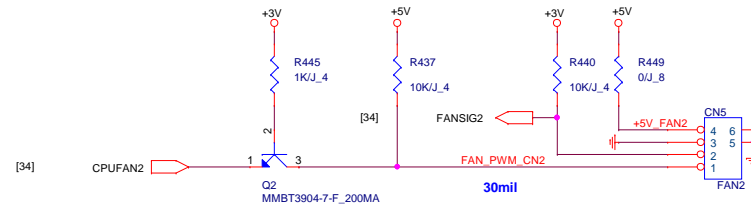
## KB\_BL LED (KBC)



## FAN1 For CPU (THM)

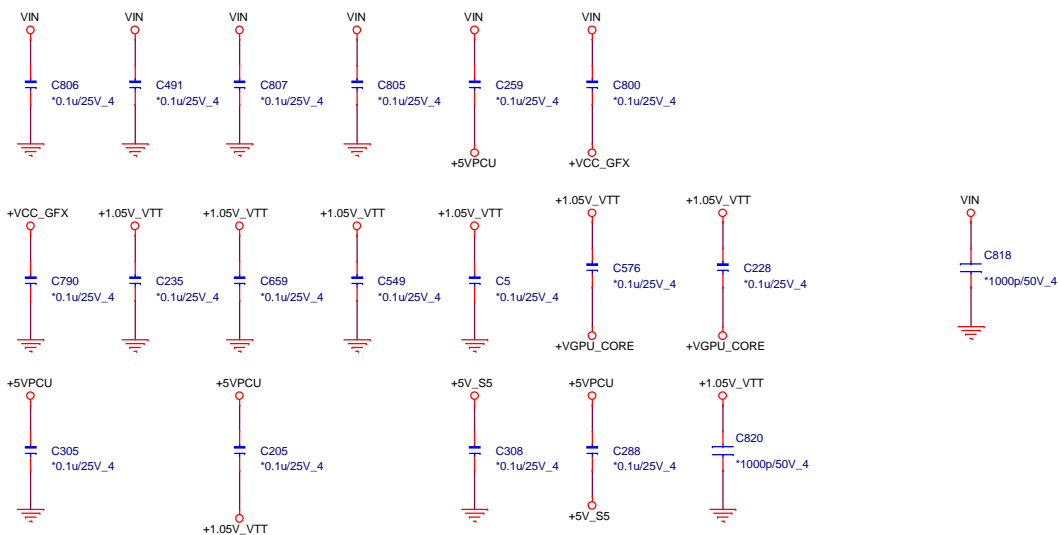


## FAN2 For GPU (THM)

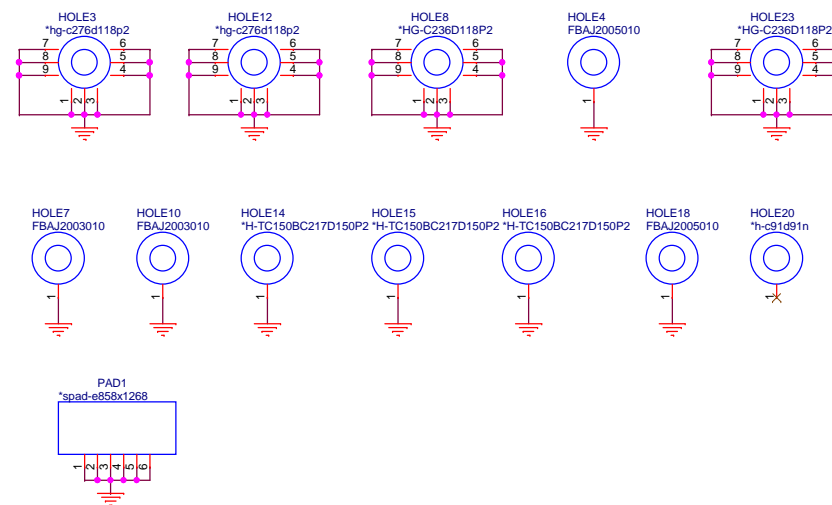
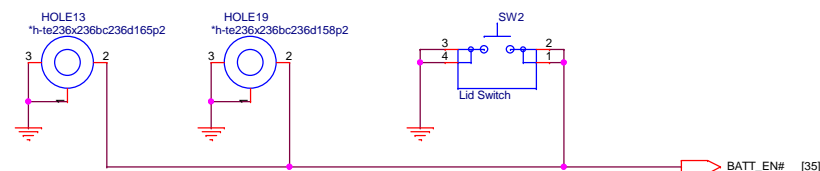




## Power LED



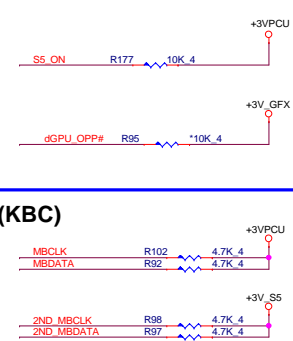
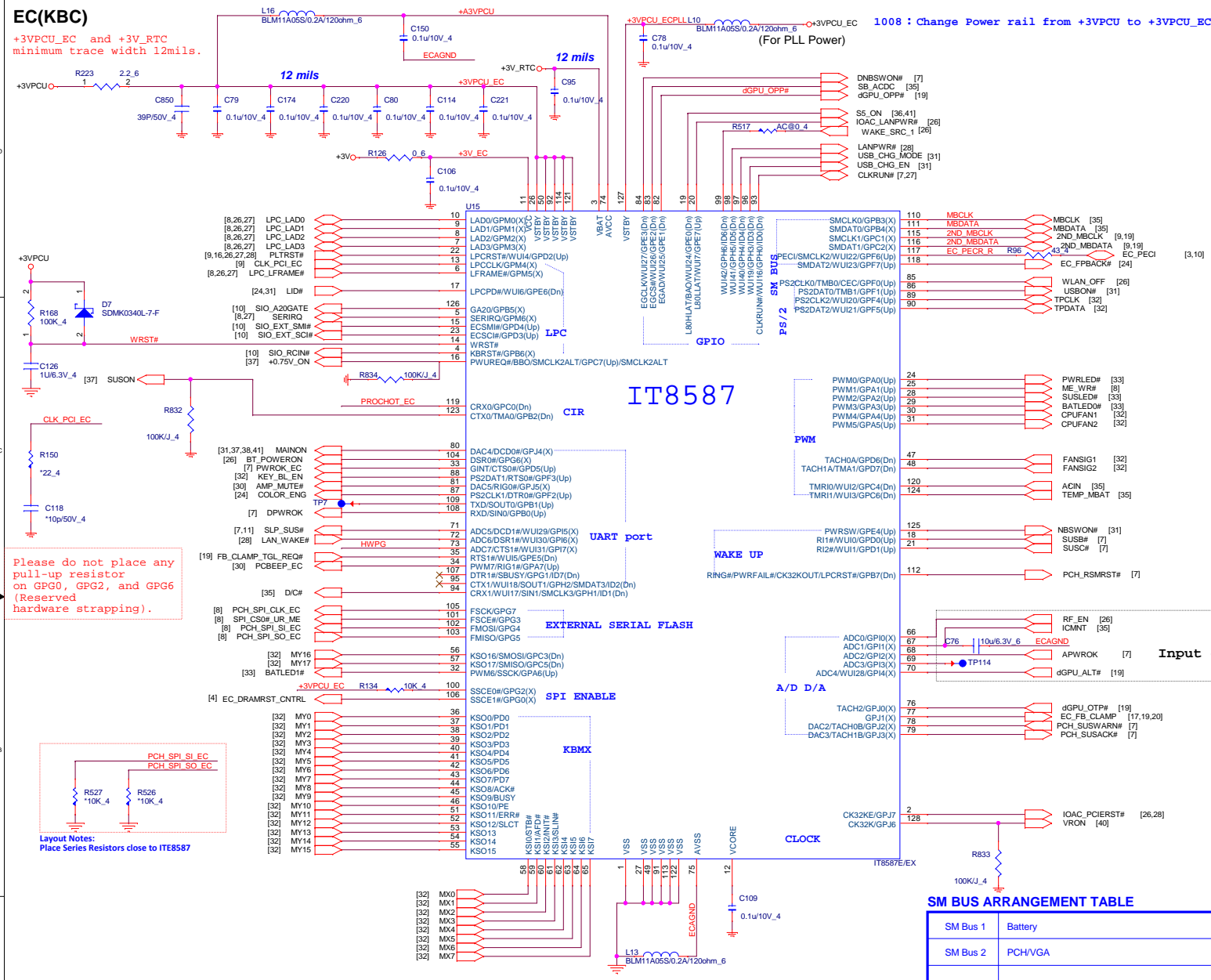
## 33



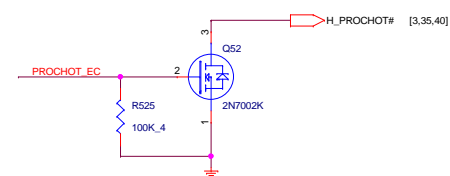
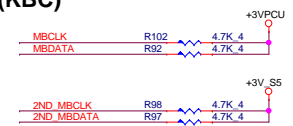


**EC(KBC)**

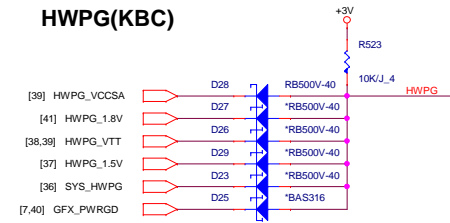
+3VPCU\_EC and +3V\_RTC  
minimum trace width 12mils.



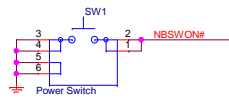
## SM BUS PU(KBC)



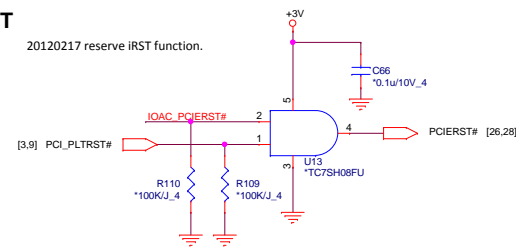
**HWPG(KBC)**



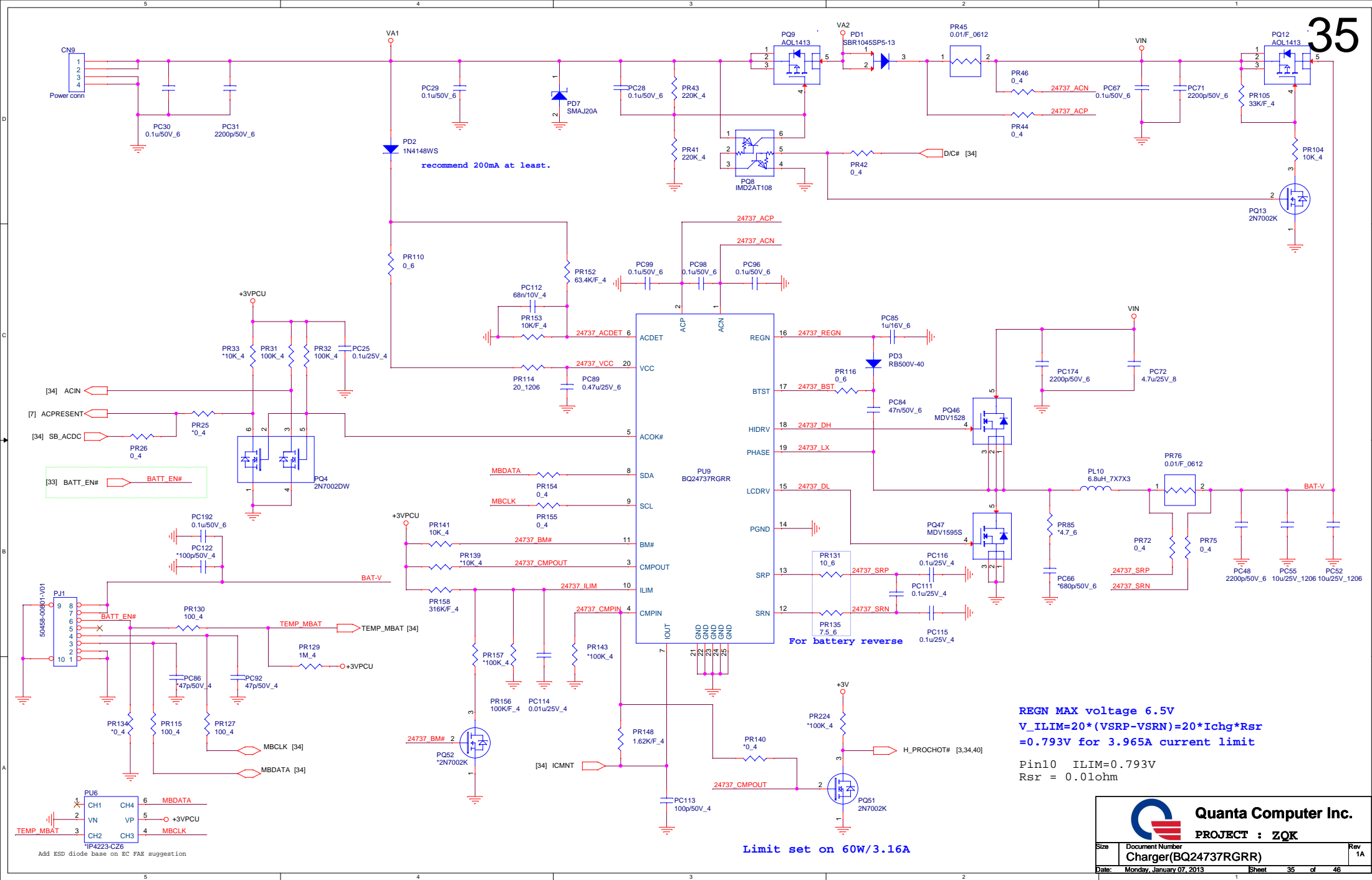
For test only

**iRST**

20120217 reserve iRST function.







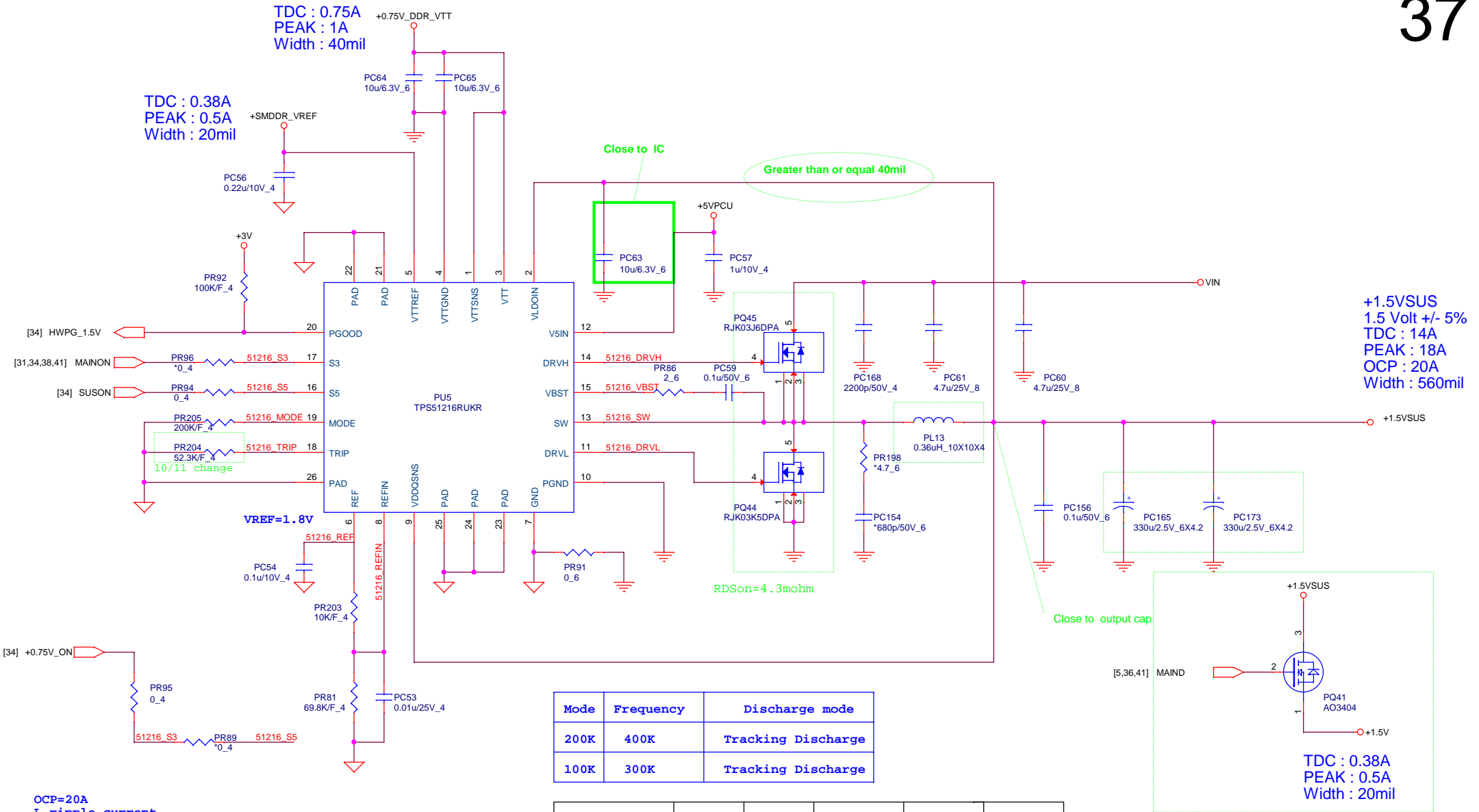






TDC : 0.38A  
PEAK : 0.5A  
Width : 20mil

TDC : 0.75A  
PEAK : 1A  
Width : 40mil



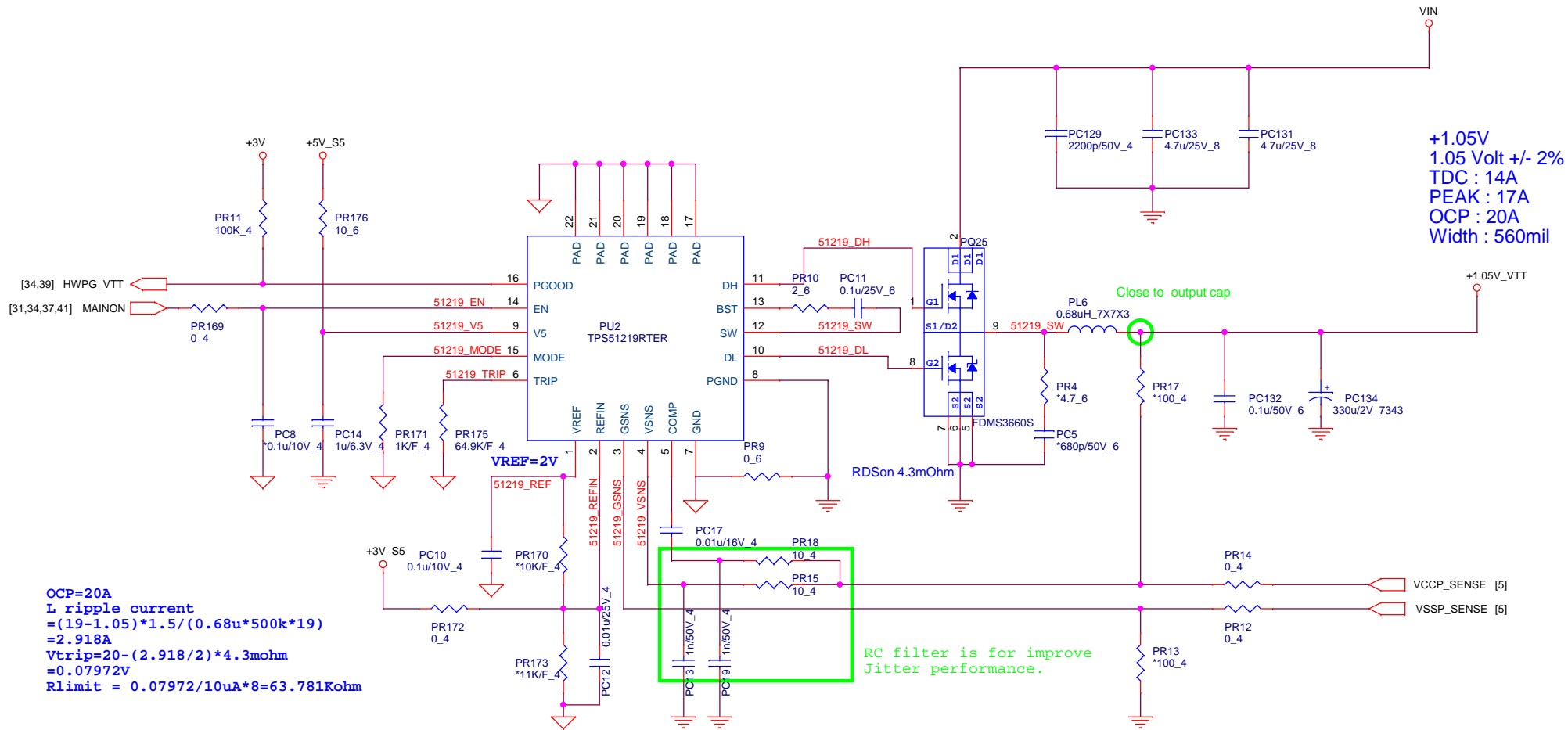
Mode	Frequency	Discharge mode
200K	400K	Tracking Discharge
100K	300K	Tracking Discharge

	S3	S5	+1.5VSUS	REF	VTT
S0	1	1	ON	ON	ON
S3 (mainon off)	0	1	ON	ON	OFF
S4/S5	0	0	OFF	OFF	OFF

**Quanta Computer Inc.**  
PROJECT : ZQK

Size: Document Number  
DDR 1.5V(TPS51216)  
Date: Monday, January 07, 2013 Sheet 37 of 46 Rev 1A

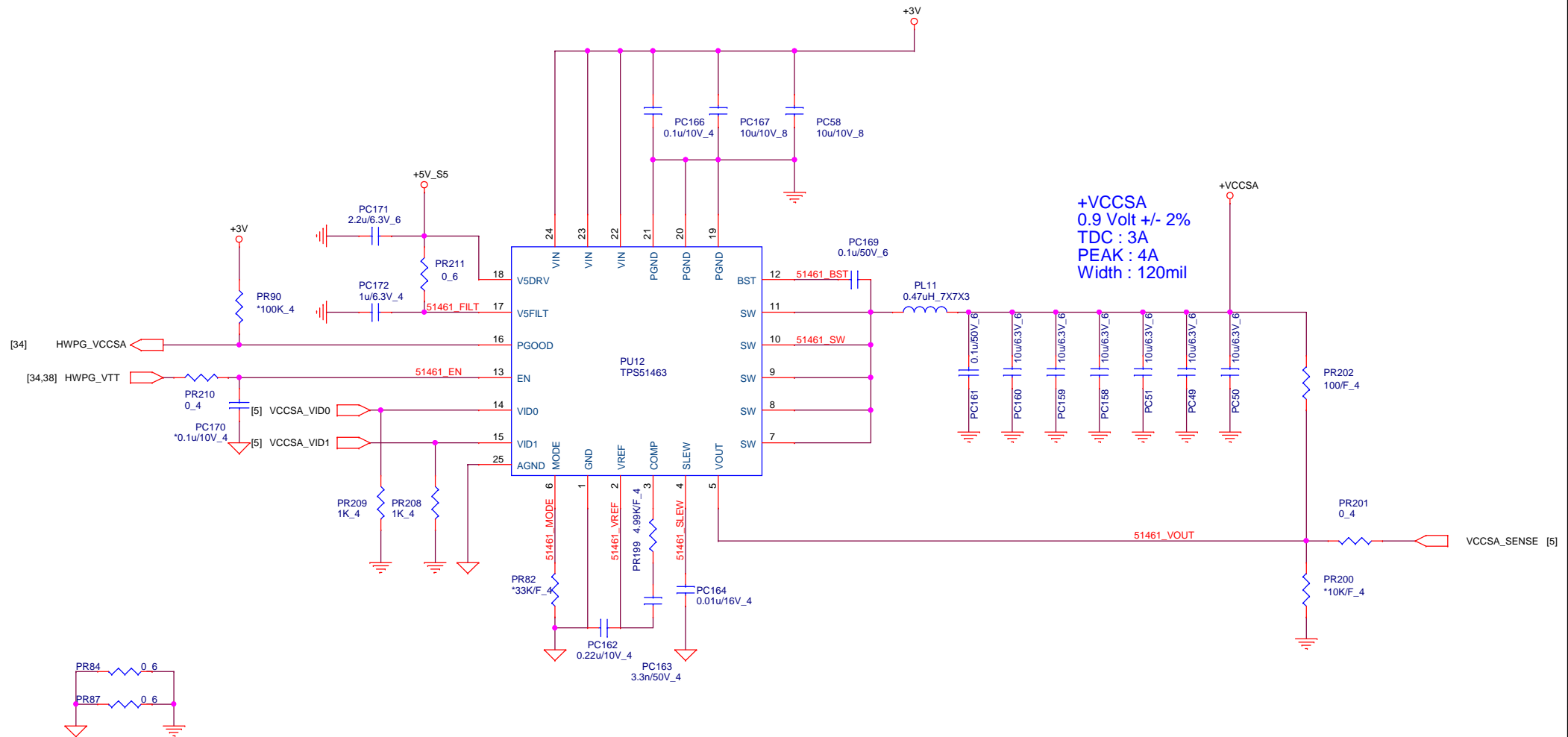




**Quanta Computer Inc.**  
**PROJECT : ZQK**

Size	Document Number	Rev
	<b>+1.05V (TPS51219)</b>	1A
Date:	Monday, January 07, 2013	Sheet 38 of 46





VID0	VID1	+VCCSA
0	0	0.9V
0	1	0.85V
1	0	0.775V
1	1	0.75V

default 0.9V

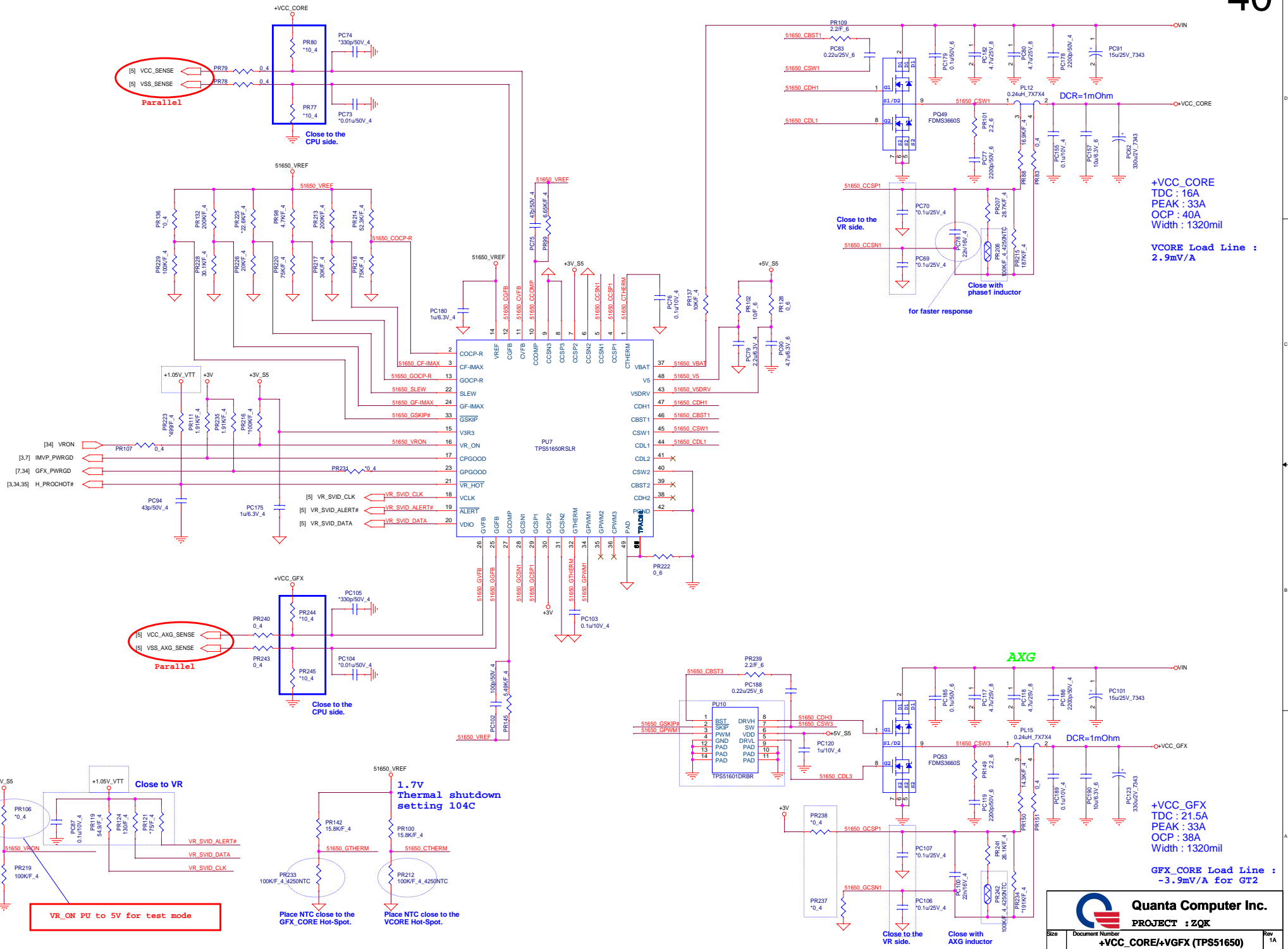


**Quanta Computer Inc.**

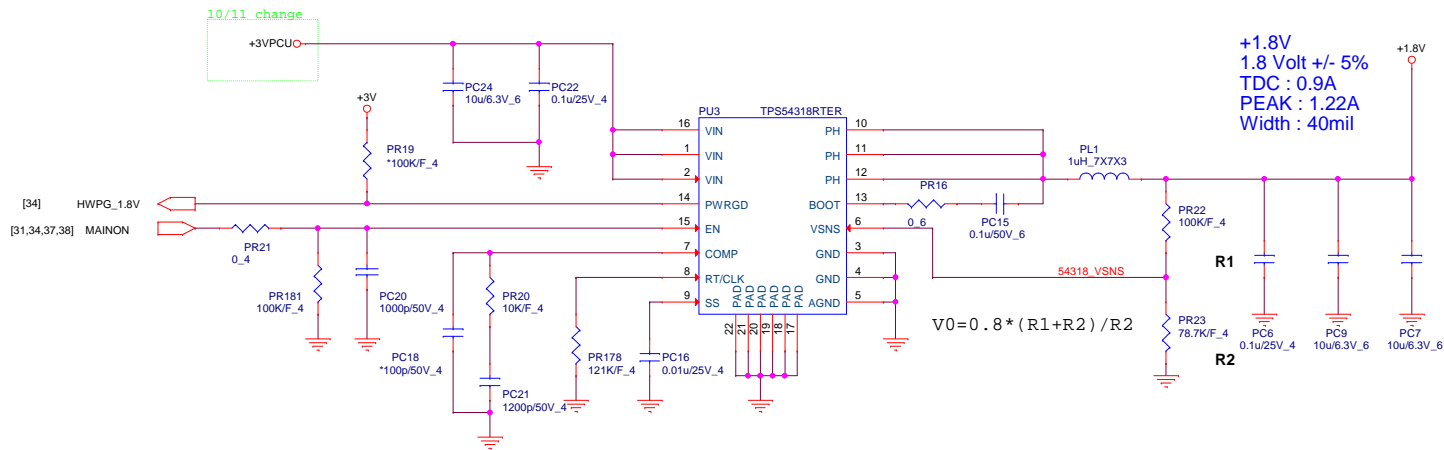
**PROJECT : ZQK**

Size	Document Number	Rev
	VCCSA(TPS51463)	1A
Date:	Monday, January 07, 2013	Sheet 39 of 46

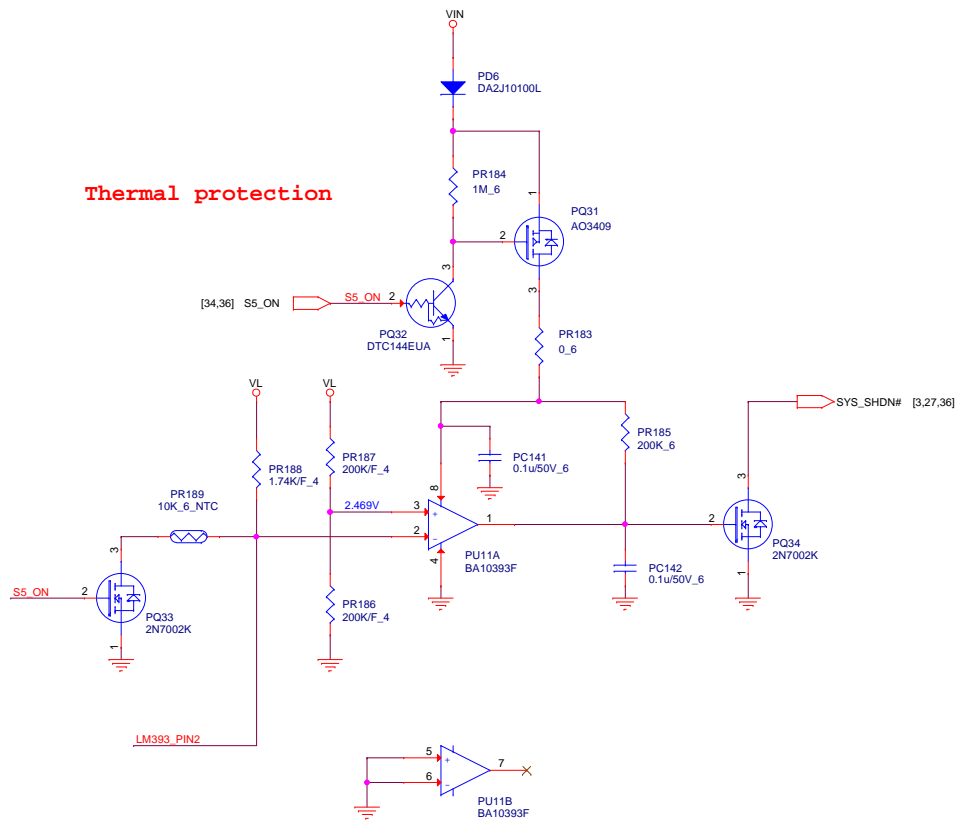




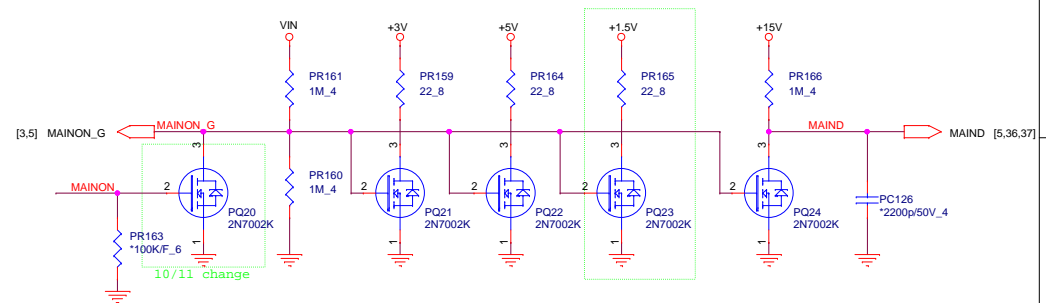




## Thermal protection



For EC control thermal protection (output 3.3V)



Quanta Computer Inc.

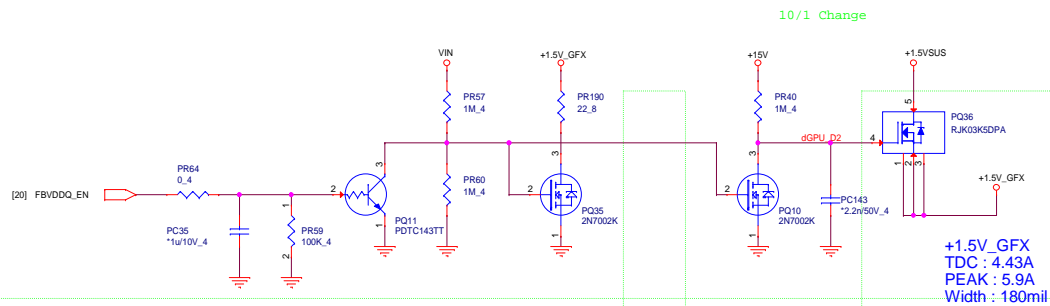
PROJECT : ZQK

Size	Document Number	Rev
		1A

+1.8V/Discharge/Thermal

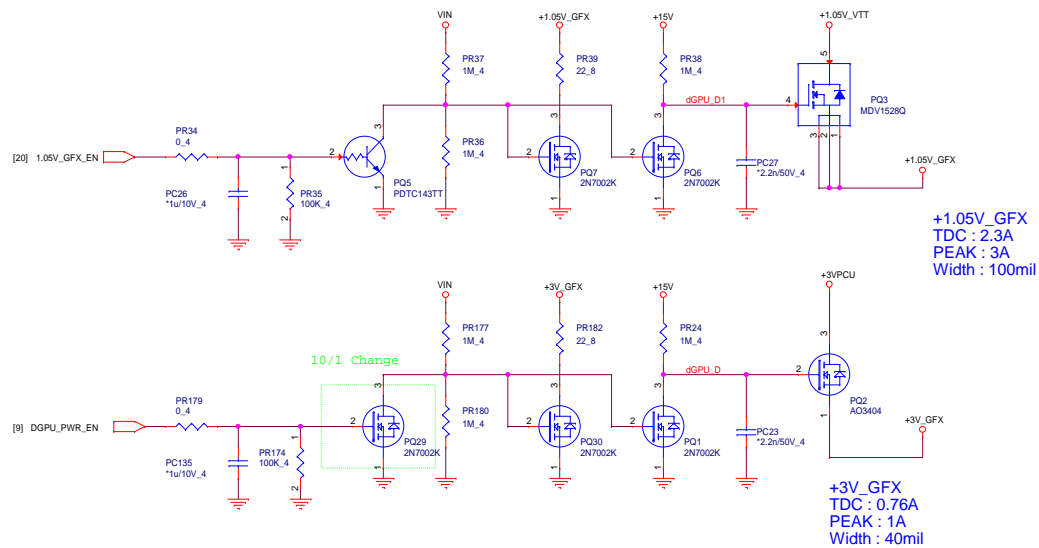
Date: Monday, January 07, 2013 Sheet 41 of 46





10/5 Reserve switching power for +1.5V\_GFX

OCP=7.5A  
L ripple current  
= $(19-1.5) \times 1.5 / (2.2 \times 290 \times 19)$   
=2.165A  
Vtrip= $7.5 - (2.165/2) \times 14 \text{mohm}$   
=0.0898V  
Rlimit= $0.0898 / 10 \mu\text{A} \times 8 = 71.873 \text{Kohm}$

















Model	Date	CHANGE LIST
ZQK	1203	1.Change C774 from 0.1uF to 39pF for ESD 2.Add C841~C850 39pF for ESD 3.Change U19,U21,U23,U26,U43,U46,U48,U49 PN from AKD5JGST404 to AKD5JGST407
	1205	1.Change LED1/LED2 PN : BEB00028ZA0 : FP : led19-123-y2st1d-c30-2t-4p 2.Change R383/R392 from 47 ohm to 56 ohm
	1206	1.Change SW2 PN : DHPATE2CK03 : FP : sw-ate-2ck-v-tr-4p
	1210	1.Delete PL2/PL3/PL4/PL5 2.Add RTC charge circiut and modify CN14 PN and FP (DFHS02FS032/ml1220-smt) 3.Update CN4 FP to "dp-adis0022-p001a-20p-smt"
	1211	1.Add mSATA re-driver circuit 2.Change CN22 PN & FP as same as CN13
	1212	1.Modify Hole4 FP to H-TC197BC142D142P2 2.Change mSATA redriver power rail to +1.5V
	1213	1.Add R828~R831 for co-layout 2.Add N14M-GE binary strap setting information
	1214	1.Change USB DB power to 4 pins 2.Change CN4 PN to DFTD20FR001
	1217	1.Update Hole6/Hole17/Hole22 FP 2.Add C866 by FAE suggestion 3.Change C706 from 10uF to 4.7uF 4.Add pull down 100K by EC-Anda command (R832/R833/R834) 5.Change TEMP_MBAT fromPJ1 pin 5 to pin 6 (BATT_EN#) , then pin 6 is NC pin 6.Un stuff PR96 7.Add R835 and change R785 to 5.1M ohm 8.Mark R746 to NSW@ due to pin18 of U7 has internal +3V
	1219	1.SUSLED# power from +3V_S5 to +3V_PCU (for Deep S3) 2.Change eDP connector CN8 PN and FP (DFHS40FS095 / gs12401-1011-40p-r-nh-smt)
	1220	1.Add net PCH_SUSWARN# connect to Pin78 of EC (GPJ2) 2.Add net PCH_SUSACK# connect to Pin79 of EC (GPJ3)
	1221	1.Change PR191 PU voltage from +3V to +3V_S5
	1224	1.Unstuff PR28/PR30 2.Reserve R837
	1225	1.Change PU4 PN from AL001642000 to AL001642001
	1226	1.Change U15 PN from AJ085870F03 to AJ085870F04
	1228	1.Co-layout mSATA re-driver IC-U51 (PS8521A & ASM1466)
	0102	1.Unstuff PR191 (Already PU on HW side) 2.Reserve R842/R843
	0103	1.SWAP EC pin : BATLED1# change to pin32 ; ME_WR# change to pin25
	0104	1.Change U38 PN from AJ0QPRG0T03 to AJSLJ8C0T05
	0107	1.Update Hole6/Hole17 FP 2.Update Pad1 PN to FBZRK011010 3.Update Hole4 PN to FBAJ2005010

		PROJECT : ZQK		DOC NO.	PROJECT MODEL :	ZQK	APPROVED BY:		DATE:
Change list					PART NUMBER:		DRAWING BY:		REVISION:
Date: Monday, January 07, 2013		By: [signature]							